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# LEC GaAS FOR INTEGRATED CIRCUIT APPLICATIONS

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**REFERENCES** 

#### LIST OF SYMBULS

GaAs Gallium arsenide

LEC Liquid encapsulated Czochralski

IC Integrated circuit

MMIC Monolithic microwave integrated circuit

CCD Charge coupled device

Si Silicon

Cr Chromium

FET Field effect transistor

III-V Three-five (columns of periodic table)

in Inch

kg Kilogram

in situ In place

TV Television

69s Six-nines (0.999999)

PBN Pyrolytic boron nitride

B<sub>2</sub>O<sub>3</sub> Boric oxide

psi Pounds per square inch

mm Millimeter

hr Hour

<111> 111 crystal axis orientation

(100) 100 crystal plane orientation

TEM Transmission electron microscopy

cm Centimeter

KOH Potassium hydroxide

°C Degrees centigrade

min Minute

EPD Etch pit density

X Magnification power

μm Micron

Se Selenium

Zn Zinc

Burger vector

Burger vector

 $\mathbf{E}_{\mathbf{g}}$  Extinction distance

E Extinction coefficient

S Bragg

SADP Selected area diffraction patterns

B/W Black and white

STEM Scanning transmission electron microscopy

θ Cone angle

SIMS Secondary ion mass spectroscopy

LVM Local vibrational mode

C Carbon

K Potassium

B Boron

S Sulfur

Te Tellurium

Mg Magnesium

Mn	Manganese
Fe	Iron
PL	Photoluminescence
meV	Milli-electron volts
<sup>p</sup> 5/2	angular momentum state with $\ell = 1$ , $J = 5/2$
<b>.</b>	Orbital angular momentum
J	Total angular momentum
г <sub>7</sub>	Symmetry label or electronic state
! <b>*8</b>	Symmetry label or electronic state
σopt	Optical cross section
ΔΕ	Full width half maximum energy of spectral feature
T <sub>D</sub>	Tetrahedral group
S <sub>3/2</sub>	Angular momentum state with $\ell = 0$ , $J = 3/2$
Cu	Copper
c <sub>3V</sub>	Point group of three-fold symmetry about in axis
B <sub>As</sub>	Boron substitutional on arsenic site
GaAs	Gallium substitutional on arsenic site
VAS	Arsenic vacancy
μ	Spherical spin orbit splitting parameter
δ	Cubic spin orbit splitting parameter
<b>ā</b>	Effective spin orbit splitting
Ai	Screening parameters
Bj	Screening parameters

Ge

GaSb

Germanium

Galium antimonide

 $Ga_{Sb}$  Gallium substitutional on antimony site

EPR Electron paramagnetic resonance

As<sub>Ga</sub> Arsenic substitutional on gallium site

EL2 Electron trap label

GaP Gallium phosphide

V<sub>Ga</sub> Gallium site vacancy

e Electron

N<sub>T</sub> Density of ionized centers

n Electron density

N<sub>ii</sub> Density of neutral centers

K Equilibrium constant

N<sub>A</sub> Shallow acceptor concentration

 $N_D$  Shallow donor concentration

 $N_A^R$   $N_A^-N_A^{carbon}$ , concentration of residual acceptors

 $N_{A}^{carbon}$  Net concentration of carbon acceptors

N<sub>EL2</sub> Concentration of EL2 deep donors

PITS Photo-induced transient spectroscopy

R-PITS PITS using rise in photocurrent

D-PITS PITS using decay

ΔI Change in current

 $I(t_1)$  Current at time  $t_1$ 

 $I(t_2)$  Current at time  $t_2$ 

e<sub>t</sub> Emission rate of trap

 $\Delta t^{-1}$  1/( $t_2$ - $t_1$ ), sampling rate

t<sub>1</sub>,t<sub>2</sub> Time

u? Type unknown

VPE Vapor phase epitaxy

HL10 Hole trap label

σ Cross section

SI Semi-insulating

EL3 Electron trap label

EL6 Electron trap label

EL7 Electron trap label

MESFETs Schottky barrier field effect transistor

JFETs Junction field effect transitor

MISFETs Metal insulator semiconductor field effect transistor

BFL Buffer field effect transitor logic

V Volts

SDFL Schottky diode field effect transistor logic

VLSI Very large scale integration

DCFL Direct coupled field effect transitor logic

A Angstrom

Si<sub>3</sub>N<sub>4</sub> Silicon nitride

Ni Nickel

Au Gold

Ti Titanium

Pt Platinum

C-V Capacitance voltage

V<sub>D</sub> Pinchoff voltage

q Elementary charge

ε Dielectric constant

W<sub>S</sub> Profile depth

 $N_d(x)$  Donor profile

x Distance

V<sub>bi</sub> Built in potential of Schottky barrier

mV Millivolts

 $\langle V_p \rangle$  Mean pinchoff voltage

 $\sigma_{V}$  Standard deviation of pinchoff voltage

Nimplant Implanted donor density

N<sub>SA</sub> Shallow acceptors in substrate

N<sub>DA</sub> Deep acceptors in substrate

N<sub>SD</sub> Shallow donors in substrate

N<sub>DD</sub> Deep donors in substrate

ICs Integrated circuits

## I. <u>Introduction</u>

Recent developments in liquid encapsulated Czochralski (LEC) techniques for the growth of semi-isulating GaAs for integrated circuit (IC) applications have resulted in significant improvements in the quality and quantity of GaAs material suitable for device processing.

The emergence of high performance GaAs integrated circuit (IC) technologies has accelerated the demand for high quality, large diameter seminisulating GaAs substrates. The new device technologies, including digital integrated circuits (ICs), monolithic microwave integrated circuits (MMICs), and charge-coupled devices (CCDs), have largely adopted direct ion implantation as the key fabrication technique for the formation of doped layers. Ion implantation lends itself to good uniformity and reproducibility, high yield and low cost; however, this technique also places stringent demands on the quality of the semi-insulating GaAs substrates.

Although significant progress has been made in developing a viable planar ion implantation technology, the variability and poor quality of GaAs substrates, particularly the commercially available Bridgman and gradient freeze GaAs materials, have hindered progress in process development.

Among the most prevalent problems have been the formation of a conductive layer at the surface following encapsulation and annealing processes, and the lack of reproducibility in implanted profiles. These effects are the result of impurity redistribution in the substrates during the thermal processing. These impurities include background levels of donors and acceptors, particularly silicon (Si) and chromium (Cr), which may be present in high con-

centrations. Due to the incorporation of silicon from the quartz boat in the gallium arsenide melt, large amounts of Cr are added to compensate these donors and produce semi-insulating materials. The Cr can redistribute during annealing, resulting in a Cr-depleted region near the surface which can be conductive, and "tails" in the profiles of shallow n-type implanted layers. The semi-insulating property of the material is the basis for device isolation in direct implant technology and necessary for the minimization of parasitic capacitances. Variability in implant profile results in poor control in the pinchoff (threshold) voltage and current through the channel of FETs. It is therefore essential to utilize thermally stable, electrically uniform and reproducible materials in GaAs device processing. High purity in these materials is desirable since substrates containing high total impurity concentrations exhibit reduced channel mobility and degraded frequency response.

The physical characteristics of GaAs substrates are equally important, with the implementation of uniform, round, large area substrates essential for the device technology to reach manufacturing. Commercial GaAs substrates grown by Bridgman or gradient freeze methods are typically limited to a maximum of 2" diameter, D-shaped wafers. Thermal gradients tend to preclude the extension of these techniques to larger substrate sizes without the formation of twins or polycrystalline regions. With the startup of production of GaAs ICs, it is essential that the standard semiconductor processing equipment, configured for large round wafers for the silicon IC industry, be utilized for cost effectiveness and yield.

The critical need for improved size, quality, and quantity of GaAs materials for integrated circuit fabrication has been the driving force for

the development of LEC techniques to produce high yield, low cost materials. In summary, these GaAs materials must exhibit:

- 1) large, uniform, round wafers
- 2) reproducible, high resistivity with thermal stability
- 3) low background impurity levels
- 4) high degree of crystalline perfection

To meet the demands of GaAs device applications, a program in the growth of GaAs crystals using the LEC technique has been initiated at this laboratory, to produce GaAs meeting the criteria described above, with high yields of single crystal, undoped semi-insulating materials. Exceptional properties for these crystals have been observed through material characterization and device processing. In this chapter, major findings of this research effort are described which have significantly affected the GaAs materials applied to the fabrication of high performance GaAs integrated circuits. Part II describes the basics of LEC growth and how this method differs from other growth techniques. In Part III, an analysis of the defects present in LEC materials is presented, together with a description of techniques to reduce the incidence of twins and dislocations in GaAs crystals. The results of detailed investigations of impurity and trapping levels are described in Part IV. A compensation model for undoped semi-insulating material based on these studies is presented, and the implications of the model for high yield growth of semi-insulating material are discussed. In Part V, the use of LEC GaAs in integrated circuit fabrication is addressed, including data on the qualification of GaAs crystals for device processing, the results of ion implantation, and the performance of digital ICs on LEC

substrates. Conclusions and implications resulting from these advances in LEC GaAs technology are outlined in the last Part VI.

## II. LEC Growth Technique

The LEC technique was first applied to the growth of PbTe by Metz et al., (1962), applied to III-V materials by Mullin et al. (1968) and adapted for use with pyrolytic boron nitride crucibles by Swiggard et al., (1977) and AuCoin et al., (1979). The LEC crystal growth facility at this laboratory has a Melbourn puller developed by Metals Research, Ltd. (see Thomas et al. this volume - Fig. 2). The resistance heated puller holds a 6-in crucible with charge-capacities up to 10 kg. The growth process is monitored through a closed circuit vidicon TV camera. The puller features in situ synthesis of the compound GaAs from elemental Ga and As. The technique eliminates the need for a separate high temperature synthesis step before crystal growth, reducing the potential for contamination.

A schematic of the LEC crucible configuration is shown in Fig. 1. The Ga and As components (69s purity) are weighed and loaded into either a high purity quartz or pyrolytic boron nitride (PBN) crucible, and topped by a preformed disc of boric oxide ( $B_2O_3$ ) with known moisture content. Except where noted otherwise, 500 g discs of  $B_2O_3$  were used, with the moisture content of hermetically sealed packages accepted as specified by the manufacturer. No additional heat treatment is used prior to growth. Charges with a total weight of  $\sim 3$  kg were used in these studies. The crystals were typically  $\sim 3$  in. in diameter, and weighed 2.5 kg. Both quartz and PBN crucibles have been successfully utilized in the growth of sem, insulating GaAs. Although the initial cost of PBN crucibles is high (generally \$4000-6 $\sim 00$ , depending on quantity and manufacturer), the crucibles can be cleaned and reused about a dozen times. The use of PBN crucibles is favored due to the higher yield of high resistivity, single crystals, as will be discussed later.

The stoichiometry of the GaAs melt can be changed by varying the composition of the charge. To make an accurate determination of the initial melt composition, it is necessary to take into account the loss of As from the charge during the heat-up cycle resulting from incomplete wetting of the  $B_2O_3$  to the crucible (particularly PBN crucibles) before synthesis. The weight loss is determined by comparing the weight of the initial charge with the weight of the crystal and the charge remaining in the crucible after the growth process. The As concentration of melts have effectively been varied from 0.46 to 0.51 atom fraction. When samples for characterization were obtained along the length of the crystal, the melt composition for each sample was determined by adjusting the initial melt composition for the crystal weight at the time of growth. The crystal weight and length are recorded during growth as a function of time.

The Ga, which is solid to just above room temperature, is loaded on top of the As so that the liquid Ga serves to encapsulate the As. Starting with a chamber pressure of 600 psi, the crucible is heated to between 450 and 500°C, at which point the  $B_2O_3$  softens, flows over the charge of Ga and As, and seals at the crucible wall. The boric oxide flows at relatively low temperatures (450°C) before significant arsenic sublimation occurs. The  $B_2O_3$  floats on top of the melt and wets the surface of the crucible and the growing crystal. The synthesis reaction ( $Ga_{1iquid} + As_{solid} = GaAs_{solid}$ ) occurs at about 800°C. The presence of the  $B_2O_3$  and the use of high argon overpressures (~1000 psi) prevent significant loss of As due to sublimination and evaporation during and subsequent to the exothermic synthesis. The GaAs melt is effectively sealed by the boric oxide, suppressing not only As loss, but also

shielding the melt against contamination from the crucible and growth ambient. The melt reaction is then allowed to equilibrate and the growth procedure begins.

Growth is initiated by dipping the seed, which is held on the pull shaft, through the transparent  $B_2O_3$  and into the melt. The seeds are generally sliced from low dislocation material. The crystal is grown by gradually withdrawing the seed from the melt. The system configuration during growth is shown in Fig. 2. The crystal diameter is gradually and controllably increased to full dimension. The seed and the crucible are rotated in the same direction at 6 and 15 rpm, respectively. The pull rate for this work was 7 mm h<sup>-1</sup> and crucible lift rate was 1.4 mm hr<sup>-1</sup>. When the growth process was terminated, the crystal was positioned above the  $B_2O_3$  encapsulating layer, and the system was cooled at a constant rate of between 30 and 80°C hr<sup>-1</sup>.

The diameter of the crystal can be controlled either by manual operation or through the use of the coracle shaper. The coracle, shown in Fig. 3, is a  $\rm Si_3N_4$  die with a round hole in the center. The coracle floats on top of the GaAs melt. A crystal pulled from the melt through the die has exceedingly good diameter control. However, the use of the coracle seems to be limited to growth in the <111> direction because other low index planes, such as (100), show a high susceptibility to twinning. In these studies, the crystal diameter was monitored manually through the differential weight signal. This signal was obtained from the "load cell," a special weighing device on which the crystal and pull shaft are mounted in the LEC system. An increase or decrease of the differential weight indicates a corresponding increase or decrease in diameter. The crystal diameter is controlled by varying the heater temperature and the

cooling rate in response to changes in the differential weight signal. The growth process is viewed continuously on the TV monitor as well to ensure stable control.

The crystals were grown in three different sections with respect to diameter, the neck, the cone, and the body, as illustrated in Fig. 4. After the seed is dipped into the melt and pulling has begun, the "neck" is formed by reducing the diameter of the crystal below the diameter of the seed (~4 millimeters) to from 1 to 3 millimeters. Then the diameter is gradually and controllably increased forming the "cone." When the diameter of the cone reaches the desired dimension, the diameter of the crystal is kept constant for the remainder of the growth run.

In the following sections, the results of studies on the impact of growth parameters, including seed quality, melt stoichiometry,  $B_2O_3$  wetness, seed necking, cone angle, and diameter control, on the crystalline and electrical characteristics of the resulting GaAs ingots are detailed.

## III. <u>Crystalline Quality</u>

The primary defects observed in LEC materials include dislocations, twins, surface Ga inclusions, and micro-defects. Preferential etching, x-ray reflection topography, and optical, infrared, and transmission electron microscopy (TEM) have been used to characterize these defects. Significant progress in improving crystalline quality through reduction of the defect concentrations in large-diameter LEC GaAs has resulted from a matrix of growth experiments. Dislocation densities below 10,000 cm<sup>-2</sup> and a single crystal yield >80 percent have been observed under the appropriate growth conditions.

In the following discussion, results are presented on the dislocation density and distribution, the reduction of dislocation density by various growth techniques, the reduction of twin formation by control over the melt stoichiometry, surface Ga inclusions, and micro-defects observed by TEM. Substantial reductions in the dislocation densities of LEC materials and in twinning incidence have resulted from studies investigating dislocation formation and distribution, cone angle, and the effects of  $B_2O_3$  height, ambient pressure, seed quality and necking, diameter control, and stoichiometry.

#### 1. DISLOCATION STUDIES

Current interest in large-diameter GaAs crystals grown by the liquid encapsulated Czochralski (LEC) technique (Fairman et al., 1981; Thomas et al., 1981) stems from the need for substrate material for digital and monolithic integrated circuit fabrication. As these circuits become larger and more complex, possible adverse effects from dislocations on device performance and reliability may appear. However, at this stage of development,

there have been virtually no systematic studies reporting the possible role of dislocations. As a first step the density and distribution of dislocations across large-diameter substrates have been characterized and the means by which these are controlled by the crystal growth process is determined. This understanding is also important for the application of large-diameter LEC material to minority-carrier devices such as solar cells, where low dislocation densities are required to achieve high minority-carrier lifetimes and diffusion lengths.

A principal cause of dislocations in bulk GaAs crystals is stress induced by thermal gradients (Penning, 1958; Mil'vidskii and Bochkarev, 1978; Jordan et al., 1980b; Jordan, 1980a) during crystal growth. Radial gradients are of particular concern in Czochralski-type growth configurations (LEC, Gremmelmaire). Most of the published dislocation studies on GaAs concern small-diameter (<0.5 inch-diameter) crystals grown by the LEC (Grabmaier and Grabmaier, 1972; Brice, 1970; Seki et al, 1978), Bridgman (Brice and King, 1966; Parsey et al., 1981) and modified Gremmelmaire (Steinemann and Zimmerli, 1946) techniques. Since gradients generally decrease as the crystal diameter decreases, "effectively" dislocation-free, small-diameter GaAs crystals have been grown (Grabmaier and Grabmaier, 1972; Seki et al., 1978, Parsey et al., 1981: Steinemann and Zimmerli, 1966). Growth parameters reported to reduce radial gradients in small-diameter LEC crystals include the height of the B<sub>2</sub>O<sub>3</sub> encapsulating layer (Grabmaier and Grabmaier, 1972; Shinoyama et al., 1980) and the cone angle (Roksnoer et al., 1977). Material properties which have been identified with the suppression of dislocations include the concentration of impurities (Seki et al, 1978, Suzuki et al., 1979; Mil'vidskii et al.,

1981) and melt stoichiometry (Brice, 1970; Brice and King, 1966; Parsey et al., 1981). Other dislocation studies for large-diameter LEC GaAs have been made by Thomas et al., this volume, Section 2 and by Hiskes et al., 1982 (see Stolte, this volume, Section 1).

Eighteen undoped crystals were grown and analyzed in this study. The crystals were sliced according to the diagram shown in Fig. 5. The samples were lapped and polished on both sides. Dislocation densities and distributions were evaluated by preferential etching (KOH for 25 min at  $400^{\circ}$ C). This etch preferentially attacks dislocations intersecting the surface of the sample, forming hexagonal etch pits. The etch pit density (EPD) corresponds directly to the dislocation density as confirmed by x-ray topography at this laboratory and elsewhere (Angilello et al., 1975). The EPD measurements were typically made from low-magnification (70X) micrographs by counting the pits over 1.3 × 1.0 millimeter regions. Higher magnification (either 140X or 280X) was required to resolve the pits when the EPD exceeded approximately  $1 \times 10^5$  cm<sup>-2</sup>. The estimated error in counting the pits on each micrograph was less than  $\pm 5\%$ .

Investigations concentrated on studying the effects of seven growth parameters on the dislocation density and distribution. These include: (1) cone angle, (2) seed quality, (3) seed necking, (4) diameter control, (5) melt stoichiometry, (6) height of the  $B_2O_3$  encapsulating layer, and (7) ambient pressure. The cone angle, defined as the angle between the wall of the cone and the horizontal, was varied from 0 to 65°. Crystals with a cone angle of 10° or less than 20° are referred to as "flat-top" crystals. The EPD of the seed crystals ranged from about  $1.5 \times 10^3$  to  $5 \times 10^5$  cm<sup>-2</sup>. Crystals were

grown with high and low EPD seeds, with and without Dash-type necking (Dash, 1957). The neck diameter varied from 1.2 to 3 mm. Diameter control refers to the deviation of the diameter from the average value. The lowest diameter deviations ( $\pm 1.1$  mm) were achieved by controlling the diameter with the cooling rate with minimal direct adjustments of the melt temperature. The initial melt stoichiometry varied from 0.462 to 0.506 As atom fraction. Procedures necessary for making an accurate determination of the melt composition have already been discussed. The height of the  $B_2O_3$  encapsulant above the melt was approximately 17 mm in the majority of the growth experiments, corresponding to 500 g of material. One experiment each was made with 170 and 390 g of  $B_2O_3$ , corresponding to 9 and 13 mm heights, respectively. The ambient pressure during growth was typically 300 psi. One experiment was conducted at a lower pressure of 50 psi (see Stolte, this volume, Section 1, for a discussion of low pressure growth).

# a. Radial Dislocation Distribution

The distribution of dislocations across wafers exhibits fourfold symemtry indicative of the <100> crystallographic orientation, as shown
in Fig. 6. The main features of the distribution are: (1) minimum EPD occurs
over a large annulus between the center and edge (Region 1, or "ring" region);
(2) intermediate EPD occurs in the center (Region 2, or "center" region); (3)
maximum EPD occurs at the edge (Region 3, or "edge" region). A microscopic
view of the dislocation distribution across wafers, as shown in Fig. 7,
clearly shows the large variations of EPD. In addition, the EPD in the ring
and edge regions is greater along the <100> than the <110> direction (see

Fig. 7). Measured EPD distributions across the full diameter of wafers typically display a "W"-shaped profile, as shown in Fig. 8.

Experimentally determined radial EPD distributions are consistent with theoretical thermoelastic analyses of Czochralski crystals of Penning, (1958) and Jordan et al., (1980a, 1980b). Jordan calculated the total stress in the crystal in terms of twelve (111) <110> slip systems. The dislocation density is assumed to be proportional to the total stress within an additive constant. Since the periphery of the crystal is cooler than the center as the crystal is pulled from the melt, the periphery and center are under tension and compression, respectively. The calculated stress is highest at the periphery, consistent with the experimental finding that the maximum EPD occurs in the "edge" region of the crystals. The calculated stress is lowest in the transition between regions of tension and compression, consistent with the fact that the lowest measured EPDs occur in the "ring" region. The relatively high EPD measured along <100> compared to along <110> is explained in terms of the theory by the fact that more slip systems contribute to the total stress along <100>. The agreement between theory and experiment indicates that radial gradient-induced stress is the principal cause of dislocations in these crystals. These results agree with other experimental studies (Jordan et al., 1980b) of (100) GaAs.

Variations in the nature of the radial distribution from the front to the tail of the crystal are discussed in Section 1-c.

### b. <u>Dislocation Networks</u>

An important morphological feature of the microscopic dislocation distribution is the formation of etch pit networks. Two types of morphologies are observed. The first is a cellular network, seen in Figs. 6 and 7, where the dislocations form an interconnected network of cells with few dislocations within each cell. The approximate diameter of the cells is 500  $\mu$ m corresponding to an EPD of 2 × 10<sup>4</sup> cm<sup>-2</sup>. The cell diameter decreases as the EPD increases (100  $\mu$ m corresponding to an EPD of about 1 × 10<sup>5</sup> cm<sup>-2</sup>). When the EPD is less than about 2 × 10<sup>4</sup> cm<sup>-2</sup>, the morphology of the network takes on a lineage structure, where the etch pits form visible wavy lines. These lines extend from a few millimeters to more than one centimeter, and are oriented along <110>, as shown in Fig. 6.

These dislocation networks may form as a result of the polygonization process (Reed-Hill, 1973) where the dislocations re-align themselves after solidification to reduce the strain energy of the crystal. The re-alignment probably occurs by both climb and glide processes. In general, dislocations in zincblend materials can undergo alignment into walls defined by (110) planes perpendicular to (111) slip planes. These walls would intersect (100) planes along <110> directions, consistent with the observations. The cellular network, in effect, constitutes a high packing density of lineage structures where one dislocation may interact with several dislocation lines, forming interconnected networks.

### c. <u>Longitudinal Dislocation Distribution</u>

The longitudinal variation (along the growth direction) of the dislocation density was examined by comparing radial distributions of wafers obtained from the front, middle, and tail of the crystals, as shown in Fig. 8. Except for the edge in ingots 9, 11, 12, and 15 as well as the center of ingot 15, the EPD invariably increased from front to tail in each of the three regions, as shown in Table I, while the radial profiles remained "W"-shaped, as shown in Fig. 8. This behavior could indicate that the overall level of stress increased along the crystal, or that the dislocations multiplied after growth, or both. The average EPD increased from front to tail (see Table I) by a factor of 8, 7, and 1.5 in the "ring," "center," and "edge" regions, respectively. Further, the ratio of the EPD in the "center" to that in the "ring" region decreased from front to tail in the majority of the crystals, as shown in the table. These results show that the radial EPD distribution becomes more uniform toward the tail of the crystals even though the "W"-shaped profile persists.

# d. Parameters Affecting Dislocation Density

In this section, results are presented concerning the quantitative dependence of the dislocation density on cone angle,  $B_2O_3$  thickness, ambient pressure, seed quality and necking, diameter control, and melt stoichiometry. The effect of each growth parameter was evaluated by determining the change in the EPD across each substrate as that parameter was independently varied. Since the EPD density in the "ring," "center," and "edge" regions represent local limits of the entire EPD distribution, the

Table I. Summary of EPD Measurements on LEC Ingots

Ingot No.	Wafer Location	(1) Ring	EPD (cm <sup>-2</sup> (2) Center	(3) Edge	EPD Ratio (Center to Ring)
1	F	7.6 × 10 <sup>4</sup>	4.6 × 10 <sup>4</sup>	$3.0 \times 10^{5}$	0.6
	T	$6.1\times10^5$			1.0
2	F	2.2 × 10 <sup>4</sup>	$5.0 \times 10^4$	2.3 × 10 <sup>5</sup>	2.3
	M	$3.2\times10^4$	$7.3\times10^4$	$2.5\times10^5$	2.3
3	F	4.0 × 10 <sup>4</sup>	$8.0 \times 10^4$	$2.9 \times 10^{5}$	2.0
	T	N/A	N/A	N/A	
4 <sup>++</sup>	F	$4.0 \times 10^4$	1.4 × 10 <sup>5</sup>	4.0 × 10 <sup>5</sup>	3.5
	М	$3.0 \times 10^4$		N/A	3.3
5	· <b>F</b> .	$1.5 \times 10^4$	$3.4 \times 10^4$	1.7 × 10 <sup>5</sup>	2.3
	T	$1.2\times10^5$	$1.4\times10^5$	$2.1\times10^5$	1.2
6	F.	$1.8 \times 10^4$	2.6 × 10 <sup>4</sup>	8.0 × 10 <sup>4</sup>	1.4
	T	$8.6 \times 10^4$	$7.7 \times 10^4$	$2.0 \times 10^5$	0.9
7	F	$1.0 \times 10^4$	2.5 × 10 <sup>4</sup>	5.6 × 10 <sup>4</sup>	2.5
	M	2.5 × 10 <sup>4</sup>	$3.9 \times 10^4$	$7.8 \times 10^4$	1.6
8	F	$1.4 \times 10^4$	$3.7 \times 10^4$	1.0 × 10 <sup>5</sup>	2.6
		N/A		N/A	
9	F	$1.4 \times 10^4$	$2.0 \times 10^4$	2.5 × 10 <sup>5</sup>	1.4
			$1.0\times10^5$		1.0

Table I (Continued)

Ingot No.	Wafer Location	/1\ 0:	EPD Ratio		
Ingut No.	Location	(1) Ring	EPD (cm <sup>-</sup> (2) Center	(3) Edge	(Center to Ring
10	F	$1.0 \times 10^4$	$2.1 \times 10^4$	$1.1 \times 10^5$	1.9
	T	N/A	N/A	N/A	•
11	F	$7.5 \times 10^3$	1.3 × 10 <sup>4</sup>	$1.9 \times 10^5$	1.7
	Ţ	$8.1 \times 10^4$	$1.8\times10^5$	$1.8\times10^5$	2.2
12	F	1.2 × 10 <sup>4</sup>	$1.7 \times 10^4$	2.5 × 10 <sup>5</sup>	1.4
	T	$9.0 \times 10^4$	$1.0\times10^5$	$2.2\times10^5$	1.1
13	F	$3.5\times10^4$	$1.0 \times 10^5$	$1.5\times10^5$	2.9
	Τ*	$8.0 \times 10^4$	$1.1\times10^5$	$2.0\times10^5$	1.1
14	F	$6.0\times10^3$	1.8 × 10 <sup>4</sup>	$9.6 \times 10^4$	3.0
	T	N/A	N/A	N/A	_
15++	F	$1.1 \times 10^5$	$2.4 \times 10^5$	2.7 × 10 <sup>5</sup>	2.2
	T	$1.3\times10^5$	$2.3 \times 10^5$	$1.6 \times 10^5$	1.8
16	F	$1.3 \times 10^4$	2.8 × 10 <sup>4</sup>	$1.7 \times 10^{5}$	2.2
	T	$1.4 \times 10^5$	$2.2\times10^5$	$2.4 \times 10^5$	1.6
17	F	1.1 × 10 <sup>4</sup>	$2.0 \times 10^4$	$1.1 \times 10^{5}$	1.8
	Ţ	$1.5 \times 10^5$	$2.5 \times 10^5$	$1.7 \times 10^5$	1.7
	F	$8.5 \times 10^3$	1.6 × 10 <sup>4</sup>	$1.2\times10^5$	1.9
18		$9.7 \times 10^4$	$1.3 \times 10^{5}$	$2.4 \times 10^{5}$	

entire distribution can be characterized with these three EPDs. Only when all three of these EPD values changed in the same direction were conclusions drawn concerning the effect of that particular growth parameter. The spatial resolution of these measurements in the center and ring regions (averaging over  $1.3 \times 1.0$  mm areas) is sufficient to reflect true variations in the average dislocation density across wafers while minimizing contributions due to microscopic fluctuations in density associated with polygonization. However, since higher magnifications were used to determine the EPD near the edge of the crystals, these measurements probably represent the true average EPD to within ±25%. Therefore, measurements obtained from the center and ring regions were more sensitive indicators of actual EPD variations from crystal to crystal than measurements from the edge. In effect, the center and ring regions weigh more heavily. (Since the center and ring measurements encompass approximately 80% of the area of a substrate, the heavier weighting of the center and ring measurements is justifiable from a practical standpoint.) The EPD values reported in the tables are an average of at least two measurements.

# (1). Cone Angle

The effect of the cone angle on the dislocation density can be evaluated by comparing the EPD of full-diameter wafers cut from the front of each crystal. The results, shown in Table II, show no correlation between cone angle and EPD for cone angles greater than about 25°. For example, crystals No. 9 and No. 10 were grown under very similar conditions in terms of the other six parameters reported in this paper. The only difference is the cone angle, which is 30° and 62° for crystals No. 10 and No. 9, respectively. The

Table II. Effect of Cone Angle on Dislocation Density

Ingot No.	Cone Angle*	**	EPD (cm <sup>-2</sup> ) Front
	10	1	1.1 × 10 <sup>5</sup>
15	0°	2	$2.4 \times 10^5$
		3	$2.7 \times 10^5$
4		1	4.0 × 10 <sup>4</sup>
4	10°	2	$1.4 \times 10^{5}$
		3	$4.0 \times 10^5$
17		1	$1.1 \times 10^4$
17	25°	2	$2.0\times10^4$
		3	$1.1 \times 10^5$
10		1	$1.1 \times 10^4$
10	30°	2	$2.1 \times 10^4$
		3	$1.1\times10^5$
6		1	$1.8 \times 10^4$
	50°	2	$2.6 \times 10^4$
		3	$8.0 \times 10^4$
9		1	$1.4 \times 10^4$
	62°	2	$2.0 \times 10^4$
		3	$2.5\times10^5$
		1	$1.4 \times 10^4$
8	65°	2	$3.7 \times 10^4$
		3	$1.0\times10^5$

<sup>\*:</sup> Other growth parameters are similar.
\*\*: 1-ring, 2-center, 3-edge (see Fig. 8).

data shows virtually no difference between the EPD values in the center and ring regions.

On the other hand, the EPD in the front of the flat-top crystal (No. 15) is in the low  $10^5~\rm cm^{-2}$  range. In addition, the longitudinal distribution is inverted along approximately the first half of the crystal, first decreasing from the front toward the tail before increasing again as in all the other crystals. The crystal began to expand rapidly when the top of the crystal emerged from the  $B_2O_3$  encapsulating layer, leaving a bulge at a distance from the front of the crystal equal to the height of the  $B_2O_3$  layer. This behavior shows that the crystal experienced significant additional cooling when emerging from the  $B_2O_3$ , indicating that the convective heat transfer from the crystal to the ambient was large compared to the heat transfer to the liquid encapsulating layer. The increased cooling presumably raised the level of stress near the top of the crystal leading to the unusually high dislocation density.

Dislocation maps of longitudinal cross sections of cones (see Fig. 9) were analyzed to follow the dislocation density distribution along the growth direction for various cone angles. The "W"-shaped radial distribution observed across wafers was clearly visible in these samples, as shown in Fig. 9. However, the longitudinal EPD increased after the neck, reached a maximum value, and then decreased before the crystal reached full diameter. (A continuous increase in EPD was expected in the cone region because the diameter expands continuously, and radial gradients typically increase as the diameter increases.) The maximum value of the EPD decreases as the cone angle increases, as indicated in Fig. 9. A high concentration of slip traces was

also observed in the cone region in crystals grown with shallow cones. In addition, the maximum of the longitudinal EPD distribution was located directly below the neck in shallow cones, and closer to the center of the high-angle cones, as is evident in Fig. 9.

The variation with cone angle of both the EPD at the maximum and the position of the maximum within the cone as the cone angle decreased from 65° to 30° is consistent with the behavior of the flat-top crystal; i.e., the maximum EPD occurred at the top of the flat-top crystal, and the EPD at the maximum was the highest of all the crystals. Evidently the same mechanism controls the dislocation density and distribution at the top of all of the crystals, the flat-top crystal representing the limiting case of a 0° cone angle. In view of the discussion earlier in this section concerning the flat-top crystal, the dislocation maximum forming as the cone emerged from the  $\rm B_20_3$  encapsulating layer is likely a result of increased convective heat transfer to the ambient. The dislocations associated with the maximum represent a "secondary" distribution added to the primary ("grown-in") distribution which formed at the solidification front.

Study of the secondary dislocation distribution suggests the following model for the heat flow in the crystal at a position corresponding to the top surface of the encapsulating layer. The isotherm shape is determined by the relative vertical and radial components of heat flow. The vertical heat flow is relatively strong when the crystal is thin (as the neck emerges from the  $B_2O_3$ ), and the isotherm shape is relatively flat. When the cone begins to emerge from the  $B_2O_3$ , radial heat flow becomes more important; the isotherm shape becomes more concave with respect to the solid as the radial gradient

increases. The radial gradient increases as the cone angle decreases, leading to more pronounced EPD maximums for shallower cone angles. As the vertical wall of the crystal begins to emerge from the encapsulating layer, the curvature of the isotherm decreases leading to reduced gradients.

### (2). $B_2O_3$ Height

By varying the height from 9 to 17 mm, the effect of the height of the  $B_2O_3$  encapsulating layer on the EPD was evaluated. The results in Table III, show that the EPD decreases in regions 1 and 2 as the height of the layer increases. The effect is more pronounced at the front of the crystals. In addition, the nature of the secondary dislocation distribution in the cone region was independent of  $B_2O_3$  height. This behavior indicates that the radial gradients near the crystal-melt interface decrease as a direct result of the presence of a thicker  $B_2O_3$  layer. In view of the results of the previors section, which showed that the heat transfer from the crystal to the ambient (above the  $B_2O_3$ ) is greater than the heat transfer to the  $B_2O_3$  liquid, apparently the reduction of the radial gradient in the crystal attributed to thicker  $B_2O_3$  layers results from more effective thermal isolation between the region of the crystal near the melt interface and the Ar ambient. This finding disagrees with the theory of Jordan et al., (1980) which predicts that the radial gradient would decrease as the  $B_2O_3$  height decreases.

Table III. Effect of  $B_2O_3$  Height on Dislocation Density

Ingot No.	Weight of <sup>†</sup> B <sub>2</sub> 0 <sub>3</sub>	**	EPD (cm Front	<sup>2</sup> ) Tail
13	270 gm		$3.5 \times 10^4$ $1.0 \times 10^5$ $1.5 \times 10^5$	$8.0 \times 10^{4}$ * $1.1 \times 10^{5}$ * $2.0 \times 10^{5}$ *
16	390 gm		$1.3 \times 10^4$ $2.8 \times 10^4$ $1.7 \times 10^5$	$1.4 \times 10^{5}$ $2.2 \times 10^{5}$ $2.4 \times 10^{5}$
12	500 gm	1 2 3	$1.2 \times 10^4$ $1.7 \times 10^4$ $2.5 \times 10^5$	$9.0 \times 10^4$ $1.0 \times 10^5$ $2.2 \times 10^5$

<sup>+:</sup> Other growth parameters are similar.  $*: \sim 3/4$  ingot length area. \*\*: 1-ring, 2-center, 3-edge (see Fig. 8)

#### (3). Ambient Pressure

One crystal (No. 14) was grown at low pressure 50 psi). EPD measurements from the front of the crystal are shown in Table IV. Excessive thermal degradation took place at the surface of the crystal due to the low ambient pressure. As a result, Ga droplets, which formed at the cone, thermally migrated through the crystal to the tail. The presence of the Ga in the crystal prevented the measurement of the EPD in the tail. The degradation, and subsequent loss of As from the crystal during growth, also prevented making an accurate determination of the melt stoichiometry. However, the electrical characteristics of the material indicated that

both the initial and final melt compositions were within the As-rich range similar to crystal No. 16. A comparison of the EPDs of the cyrstal grown at low pressure and crystal No. 16 shows that the EPD of crystal No. 14 was lower throughout, as shown in Table IV, indicating that the use of lower ambient pressures is effective in reducing the EPD. In fact, the EPD of 6000 cm<sup>-2</sup> in the ring region was the lowest value achieved in this study.

Table IV. Effect of Ambient Pressure on Dislocation Density

	Ambient		EPD (cm <sup>-2</sup> )		
Ingot No.	Pressure*	**	Front	Tail	
		1	$6.0 \times 10^{3}$		
14	50 psi Ar	2	$1.8 \times 10^4$	N/A <sup>+</sup>	
		3	$9.6 \times 10^4$		
		1	1.3 × 10 <sup>4</sup>	$1.4 \times 10^5$	
16	300 psi Ar	2	$2.8 \times 10^4$	$2.2 \times 10^5$	
		3	$1.7 \times 10^5$	$2.4\times10^5$	

<sup>\*:</sup> Other growth parameters are similar.

The results reported in Sections 1-d of this chapter indicate the importance of conventive heat transfer via the ambient in controlling the dislocation density. The heat transfer coefficient of the crystal-ambient surface is expected to increase as the square root of the pressure according to Jordan et al., (1980a,1980b). Therefore, a reduction in heat transfer by no more than a factor of 2.5 would be expected for reducing the pressure from 300 to 50 psi. The experimental finding of a 50% reduction in EPD is consistent with the theoretical prediction.

<sup>+:</sup> Not available (see text).

## (4). Seed Quality and Necking

A series of experiments determined the effectiveness of the seed quality and the Dash-type necking procedure in reducing the EPD by growing crystals from high-and-low EPD seeds with and without thin necks. The crystals were evaluated by comparing the EPDs in the front of each crystal at full diameter. The results, given in Table V, show that low-EPD crystals (EPD  $\langle 2.5 \times 10^4 \text{ cm}^{-2} \rangle$ ) can be grown by employing low-EPD seeds with and without necking as well as by employing high-EPD seeds with necking.

To understand the effect of seed necking, longitudinal cross sections of crystals in the neck region were examined. Grown-in EPD in this region could not be directly observed for neck diameters of less than about 2.5 mm because the neck region apparently deformed under the weight of the crystal, as shown in Fig. 10. However, dramatic reductions in EPD were observed for necks between about 2.5 and 3.5 mm in diameter, as shown in Fig. 10. These results indicate that the Dash-type necking procedure indeed works to reduce the dislocation censity independent of the EPD of the seed. Yet, the effect was registered in the first full-diameter wafer only for high EPD seed. This behavior can be interpreted to mean that dislocations can be transmitted from the seed to the crystal, and the transmission is reduced by necking. However, the effect of necking is limited since dislocations will be generated in the crystal even if the seed is perfectly dislocation free.

Table V. Effect of Seed Quality and Necking on Dislocation Density

Ingot No.	Necking*	EPD ( Seed	cm <sup>-2</sup> )	Tail
			1	7.6 × 10 <sup>4</sup>
1	No	H <b>i</b> gh	2	$4.6 \times 10^4$
		(5 × 10 <sup>4</sup> )	3	$3.0\times10^5$
			1	$1.5 \times 10^4$
5	Yes	High	2	$3.0 \times 10^4$
		(5 × 10 <sup>5</sup> )	3	$1.7 \times 10^5$
			1	$1.4 \times 10^4$
9	Yes	Low	2	$2.0 \times 10^4$
		$(3.3 \times 10^3)$	3	$2.5\times10^5$
			1	$1.3 \times 10^4$
16	No	Low	2	$2.8 \times 10^4$
		$(4.5 \times 10^3)$	3	$1.7 \times 10^5$

<sup>\*:</sup> All cone angles  $>25^{\circ}$  and other growth parameters are similar. \*\*: 1-ring, 2-center, 3-edge (see Fig. 8).

#### (5). Diameter Control

It is known that good diameter control favors lower dislocation densities. Some of the data on the 3-inch GaAs crystals support this view although a more definitive statement cannot be made because of the limited data. Crystals No. 6 and No. 9 in Table VI were grown under very similar conditions, except that the diameter deviation was smaller in No. 6. Note that the EPDs in the front of No. 6 are higher than in the front of No. 9, whereas the EPDs in the tail are lower. The lower EPD in the tail of

Table VI. Effects of Melt Stoichiometry and Diameter Control on Dislocation Density

Ingot No.	Initial Melt* Composition	Diameter		EPD (cm <sup>-2</sup> ) Front*** Tail	
		Variation (mm)	**	Front***	Tail
			1	$1.4 \times 10^4$	
8	53.0% Ga	± 4.0	2	$3.7 \times 10^4$	N/A
			3	$1.0\times10^5$	
	<b>-</b> 4		1	$1.8 \times 10^4$	8.6 × 10 <sup>4</sup>
6	51.5% Ga	± 3.0	2	$2.6 \times 10^4$	$7.7 \times 10^{4}$
			3	$8.0 \times 10^4$	2,2 × 10 <sup>5</sup>
	<b>.</b>		1	$1.4 \times 10^4$	1.0 × 10 <sup>5</sup>
9	51.5% Ga	± 7.1	2	$2.0 \times 10^4$	$1.0 \times 10^{5}$
			3	$2.5 \times 10^5$	$2.4 \times 10^5$
10	· · · · · · · · · · · · · · · · · · ·		1	$1.1 \times 10^4$	
	50.7% Ga	± 4.5	2	$2.1 \times 10^4$	N/A
			3	$1.1 \times 10^5$	
			1	$1.5 \times 10^4$	$1.2 \times 10^5$
5	Stoichiometric	± 8.5	2	$3.0\times10^4$	$1.4 \times 10^5$
			3	$1.7 \times 10^5$	$2.1 \times 10^5$
10			1	$1.2 \times 10^4$	$9.0 \times 10^4$
12	50.1% As	± 1.6	2	$1.7 \times 10^4$	$1.0 \times 10^5$
			3	$2.5 \times 10^5$	$2.2\times10^5$
16			1	$1.3 \times 10^4$	$1.4 \times 10^5$
	50.3% As	± 1.5	2	$2.8 \times 10^4$	$2.2 \times 10^5$
			3	$1.7 \times 10^5$	$2.4 \times 10^5$
11			1	$7.5 \times 10^3$	$8.1 \times 10^4$
	50.6% As	± 1.5	2	$1.3 \times 10^{4}$	$1.8\times10^5$
	ngles >25° and off		3	$1.9 \times 10^{5}$	$1.8 \times 10^{5}$

<sup>\*</sup> All cone angles >25° and other growth parameters are similar.
\*\* 1-ring, 2-center, 3-edge (see Fig. 8).
\*\*\* Diameter control should have no effect on front EPD.

No. 6 is attributed to the improved diameter control. Note, however, that the effect of diameter control is much less pronounced compared to that of cone angle, seed quality, and seed necking. Apparently crystals with more unstable diameter control were subjected to greater transient gradient-induced stress, which resulted in higher EPDs.

## (6). Melt Stoichiometry

The effect of melt stoichiometry on the dislocation density was studied by growing crystals from stoichiometric and non-stoichiometric melts. No correlation between EPD and melt stoichiometry was evident for Gaor As-rich melts with compositions less than 0.503 As atom fraction, as shown in Table VI. However, the growth conditions and physical parameters of crystals No. 11 and No. 12 are nearly identical except for the melt composition. Yet, the EPD values in the front of crystal No. 11 are significantly lower compared to crystal No. 12. The reduced EPD values in the front of the crystal would indicate that the As-rich melt favors reduced dislocation densities for melt compositions greater than about 0.505 As atom fraction. No significant improvement is apparent in the tail of No. 11, possibly suggesting that a small range of melt compositions between 0.505 and 0.535 provides for optimal EPD reductions.

# 2. SINGLE CRYSTAL YIELD (TWINNING)

A major problem which can affect the yield of GaAs material suitable for device processing is the incidence of twin formation. Twinning causes changes in the crystallographic orientation of the material and can

also lead to polycrystallinity and the formation of grain boundaries. Therefore, twinning must be prevented in the crystal growth process to achieve a high yield of 100-percent single-crystal wafers for device processing. Control over the melt stoichiometry was found to be important to prevent twin formation in large-diameter, undoped, <100> GaAs crystals grown by the liquid encapsulated Czochralski (LEC) technique.

Twenty GaAs crystals were grown from stoichiometric and non-stoichiometric melts to study this phenomena. The results of this study, summarized in Table VII, show that the incidence of twinning is significantly reduced when crystals are grown from As-rich melts. Only 4 of 12 (33%) crystals grown from Ga-rich melts were single. On the other hand, 7 of 8 (88%) crystals grown from As-rich melts were single. Furthermore, the incidence of twinning could not be correlated with other growth parameters, such as the wetness of the  $\rm B_2O_3$  (AuCoin et al., 1979) the cone angle (see Table VI), or fluctuations in the diameter of the crystal. The results indicate a sharp increase in twinning probability on the Ga-rich side of the stoichiometric composition.

Previous studies (Steineman and Zimmerli, 1963; Bonner, 1980) have shown that the incidence of twinning in small-diameter GaAs crystals can be reduced by growing with gradual cones; i.e., large cone angles. No correlation was evident in this work between the incidence of twinning and cone angle in large-diameter crystals. Moreover, the significantly reduced incidence of twin formation experienced using As-rich melts in the present study was achieved with small cone angles ranging from 0 to 35°.

Table

**************************************	MARKA 40-40-40-40-40		
Crystal	Crucible		
No.	Material		
Ga-rich			
1	PBN		
2	н		
3	1)		
5	#4		
6	88		
7	(1)		
8	Quartz		
9	H		
10	H		
11	u		
12	H		
As-rich	-		
13	PBN		
14	H*		
15	, W		
16	11		
17	U		
18	H		
19	H		

20

<sup>+160-500</sup> ppm H<sub>2</sub>0 in

<sup>\*</sup>Calculated melt con the growth of the 1 (final) of the crys (1)

<sup>\*\*</sup>Melts prepared in a mear-stoichiometric sa

Growth experiments employing quartz crucibles were not conducted with As-rich, undoped melts to compare with the results obtained with the Ga-rich melts. However, recently several crystals were grown with Se, Si, and Zn doping from As-rich melts using quartz crucibles. The incidence of twin formation was very low in this series of experiments (8 out of 9 crystals were single), indicating that twin formation is independent of the type of crucible material used.

The twinned crystals were categorized according to the twin morphology. One group was characterized as having only one longitudinal twin, which nucleated at the surface of the crystal and cut the crystal obliquely on a (111) plane. The twinned region of one such crystal was found by x-ray analysis (Lind, private communication) to be oriented with the <122> direction parallel to the growth direction. The secend group of crystals contained multiple twins. Twins in all crystals invariably nucleated at one of the four peripheral facets that run axially along the crystals. (The peripheral facets result from the intersection of (111) As and (111) Ga facet planes with the edge of the crystal along <110> directions that are perpendicular to the <100> growth axis). No preference was observed for either As or Ga peripheral facets as nucleation sites for twins.

The reduced incidence of twin formation in As-rich melts has been reported for GaAs grown by the Bridgman (Weisberg et al., 1962) and modified Gremmelmaier (Steinemann and Zimmerli, 1963) techniques. The consistent effect of melt stoichiometry on twin formation in GaAs grown by three different techniques would therefore seem to reflect a fundamental behavior of the material. The dramatic variation in the incidence of twinning over a

relatively small range of melt compositions observed in the present study suggests that the stoichiometry of the solid at the growth interface could play an important role. Thus, the variable resistance of the crystal to twin formation could be related to different solidification kinetics depending on whether vacancies, interstitials, or antisite defects are incorporated into the solid.

#### 3. SURFACE Ga INCLUSIONS

Small (0.1-to 1-mm diameter) Ga droplets, observed around the edges of a depth of up to about 2 mm, form as a result of the preferential evaporation of As from surface of the crystal during growth. The penetration is due to the thermal migration of the droplets from the cooler surface to the hotter interior. The direction of motion was downward, rather than horizontal, which has been confirmed by infrared microscopy. In general, dislocation clusters are formed around surface Ga inclusions; small fissures, developing from very large Ga inclusions, could eventually cause cracking of a wafer.

Significant penetration of Ga droplets is observed to occur only when the diameter of the crystal increased markedly. Therefore, good diameter control precludes the penetration of Ga inclusions and also prevents wafer damage. However, the centerless grinding technique appears to be the best way to remove all surface Ga inclusions, as well as the edge region with the highest dislocation density.

### 4. TEM OBSERVED MICRODEFECTS

Trane ission electron microscopy was used to examine the microstructure of undopen and Cr-doped LEC GaAs grown under different stoichiometric conditions. A chemical jet etching technique using 10HCl:1H<sub>2</sub>O<sub>2</sub>:1H<sub>2</sub>O etching solution was applied to produce thin foils less than 4000Å thick. Figure 11 shows bright-field (BF) TEM micrographs obtained from these wafers, indicating material free of stacking faults, low-angle grain boundaries, and dislocation loops. However, a few dislocations, as well as some black-and-white microstructures with diameters of ~80Å, are observed.

## a. Dislocations

Figure 12 shows the bright field contrast micrographs of the dislocations observed by TEM in typical LEC GaAs samples. The dislocation densities in these samples are in the range of  $10^4$ - $10^5$ /cm². These values are consistent with etch pit density values measured by preferential etching techniques. Preliminary TEM analyses using  $\frac{1}{9} \cdot \frac{1}{9} = 0$  criteria have shown that the Burger vectors for these dislocations are 1/2 [110], which are typical for the dislocations observed in crystals with the face-centered cubic structure. Further, as shown in Fig. 12(b), a precipitate with a size  $\sim 500$ Å, which is entangled with dislocations, can be observed in a sample grown from the Asrich melt (No. 11T, 53.6-percent As). The nature of the precipitate is still unknown. However, a similar defect has been reported in LEC or Bridgman-grown GaAs materials and confirmed to be an As precipitate (Cullis et al., 1980).

### b. Black-and-White Contrast Microstructures

Black-and-white (B/W) contrast microstructures, with sizes ~80A have been observed in 3" diameter, Cr-doped LEC material. Similar B/W microstructures with sizes ~80A [as in Figs. 11(a) and (b)], are observed in all undoped LEC crystals grown from Ga-rich, near-stoichiometric, or Asrich melts in quartz or PBN crucibles. The estimated density for these B/W microstructures is about  $10^{16}$  cm<sup>-3</sup>. Figures 11(a) and (b) show two special features: (1) the B/W microstructures exhibit good contrast only in thin regions of the foil (<1500Å thickness ~3  $\xi_g,$  where  $\xi_g$  is the extinction distance); and (2) the image depends sensitively on foil thickness under anomalous absorption conditions (i.e., s = 0, no deviation from the Bragg reflection condition). Optimum contrast is obtained in a narrow region at the front of the first or second dark thickness fringe. The microstructures are bright (white) at the front of the dark contour (thinner region), and dark (black) at the front of the bright contour (thicker region). Since no fine structure was observed in selected area diffraction patterns (SADP), which would have indicated the presence of precipitates, these B/W microstructures are probably due to cavities. However, additional TEM analysis and further microanalysis using Scanning Transmission Electron Microscopy (STEM) are required to confirm such predictions.

### 5. CONCLUSIONS ON CRYSTALLINE QUALITY

The density and distribution of dislocations have been characterized in 3-inch diameter LEC GaAs crystals. The radial distribution across wafers is "W" shaped, indicating excessive thermal gradient-induced

stress as the primary cause of dislocations as predicted on the basis of the models of Penning (1958) and Jordan et al. (1980a,1980b). The dislocation density along the crystals increases from front to tail at full diameter, indicating that the level of stress in these crystals increases as the crystal is pulled from the melt, or that the dislocations multiply after growth. The radial EPD distribution becomes more uniform toward the tail of the crystals even though the "W"-shaped distribution prevails. Jordan et al., (1980b) noted that a more "diffuse" radial dislocation distribution could result from the movement of 60-degree dislocations out of their slip planes into the next-to-grow layer of the crystal, adding to the glide dislocations at the solidification front. This explanacion would seem to be a reasonable basis for modelling the observed behavior.

The dependence of the dislocation density on seven crystal growth parameters was determined, with the following findings. The EPD of the full-diameter crystal is virtually independent of the cone angle 0 for 20° < 0 < 70°. However, the EPD increases significantly for 0° < 0 < 20°. Analysis of the longitudinal dislocation distribution within the cone region further shows that the EPD inverts for 20° < 0 < 70°, first increasing, and then decreasing from front to tail before the crystal expands to full diameter. These findings can be explained in terms of the dominant role played by convective heat transfer from the crystal to the ambient gas as the crystal emerges from the B203. In practical terms, these results show that crystals can be grown with a minimum dislocation density using a cone angle of about 30°. The use of 30° cone angle maximizes the number of low-dislocation wafers that can be obtained from crystals while minimizing the time required to grow the cone.

The dislocation density in the front of the crystals is found to be a relatively strong function of the height of the encapsulating layer, decreasing as the layer height increases. This effect is a direct result of a reduction in the radial gradients in the crystal near the solidification front. One possible explanation for this effect is that thicker  $B_2O_3$  layers more effectively insulate the growth interface from the ambient gas, reducing the radial gradient.

Studies reveal that Dash-type seed necking procedure is effective in reducing the dislocation density only when the EPD of the seed is high (\$\geq 5000 \text{ cm}^{-2}\$); low dislocation crystals were grown with poor quality seeds with necking, and with high quality seeds with and without necking. These results indicate that dislocations indeed transmit from the seed to the crystal, and necking greatly reduces this effect. However, the mechanism can have only a limited effect, since dislocations are generated in the crystal even if the seeds were perfectly dislocation-free. Additional reductions in the dislocation density in LEC crystals (achieved by altering the present thermal configuration) will require higher quality seeds if the necking procedure were to be eliminated from the growth process. The elimination of necking through careful selection of seeds would be advantageous from the practical standpoint of minimizing the time required to grow a crystal.

Good diameter control and the use of slightly As-rich melts favor reduced dislocation densities. However, these effects are small compared to those of the cone angle,  $B_2O_3$  height, seed quality and necking. Further work is needed to understand the effect of the melt stoichiometry.

The experimental results presented concerning the effect of cone angle,  $B_2O_3$  height, and ambient pressure indicate the influence of relatively high convective heat transfer at the crystal-ambient surface compared to the crystal- $B_2O_3$  surface. These findings disagree with theoretical predictions of the relative heat transfer coefficients. Reconciliation of this discrepancy between theory and results is needed for a better understanding of the LEC crystal growth process and further reductions of the dislocation density.

The incidence of twin formation in large-diameter, undoped, <100> LEC GaAs is reduced when the melt composition is slightly As-rich. In view of the potential for the loss of As from the charge when using in situ synthesis, the yield of single, <100> crystals will depend on close control of the melt composition. Finally, the results suggest that the barrier to twin formation is related to the stoichiometry of the solid at the solidification front.

# IV. Impurity and Defect Analysis

To evaluate purity of LEC GaAs, and to establish a model for the compensation mechanism in the undoped semi-insulating material, the principal impurities and electrically active centers were characterized and correlated with the crystal growth conditions.

#### 6. CHEMICAL PURITY

The chemical impurities were determined by secondary ion mass spectrometry (SIMS) and localized vibrational mode far-infrared spectroscopy (LVM). SIMS, a chemically specific micro-analytical technique, is particularly well suited to determining the concentration of transition metals and shallow donors in GaAs. The SIMS measurements for these crystals were made by Charles Evans and Associates, San Mateo, CA. LVM, an optical absorption technique, is useful for identifying low-atomic-number impurities in GaAs, e.g., carbon. Carbon ( $^{12}$ C) induces a local mode absorption at 582 cm $^{-1}$  at 77K; the integrated intensity of the absorption is proportional to the carbon concentration. The LVM measurements were made at 77K.

Average impurity concentrations for LEC material grown from quartz and PBN crucibles are shown in Table VIII. Results obtained from Cr-doped semi-insulating GaAs grown by the Bridgman method, which had passed material qualification procedures for GaAs integrated circuit processing, are shown for comparison.

The principal impurities found in LEC GaAs are carbon, silicon, and boron. The carbon concentration is lowest (on average) in LEC GaAs grown from

Growth
Technique Crucible
LEC Quart;

LEC

PBN

Bridgman (Cr-Doped)

Quart:

\*ND: not determined.

quartz crucibles, ranging from non-detectable limits ( $< 2 \times 10^{15} \text{ cm}^{-3}$ ) to about  $9 \times 10^{15} \text{ cm}^{-3}$ . LEC GaAs grown from PBN crucibles always contains carbon, with concentrations between  $2 \times 10^{15}$  and  $1.5 \times 10^{16} \text{ cm}^{-3}$ . High carbon levels ( $\sim 2 \times 10^{16} \text{ cm}^{-3}$ ) are detected when the coracle shaper is used, indicating contamination directly from the coracle. Carbon has not been detected in the Bridgman material studied for comparison.

Si is present in the range of  $5\times10^{14}$  to  $3\times10^{16}$  cm<sup>-3</sup> in quartz grown LEC material. On the other hand, the Si concentration of PBN grown material is consistently at the  $1\times10^{15}$  cm<sup>-3</sup> level or lower. No Si contamination from the coracle, which is made from Si<sub>3</sub>N<sub>4</sub>, seems to occur. In comparison, the Si concentration in Bridgman material is consistently in the low  $10^{16}$  cm<sup>-3</sup> range, about one order of magnitude higher than LEC PBN-grown material.

The boron concentration in LEC GaAs varies from  $1\times 10^{14}$  to  $2\times 10^{17}$  cm<sup>-3</sup>. This result is independent of the crucible material, indicating that the source of boron is the B<sub>2</sub>O<sub>3</sub> encapsulating material. Although boron is the predominant chemical impurity, boron is iso-electronic with Ga, and no evidence has been found in these investigations to indicate that boron is electrically active. The boron concentration in Bridgman material is very low (<2 ×  $10^{14}$  cm<sup>-3</sup>).

The large variations in the concentrations of both silicon and boron in LEC material are explained in terms of the effect of the "wetness" of the  $B_2O_3$  encapsulant: the Si and B concentrations both decrease as the water content of the  $B_2O_3$  increases, as shown in Fig. 13. The Si concentration

decreases from the low  $10^{16}$  cm<sup>-3</sup> range to below 1 ×  $10^{15}$  cm<sup>-3</sup> as the water concentration in the  $B_2O_3$  increases from about 200 to 1000 ppm. The boron concentration decreases from the low  $10^{17}$  cm<sup>-3</sup> range to below 1 ×  $10^{15}$  cm<sup>-3</sup> with the same change in water level.

The dependence of the Si concentration on  $B_2 O_3$  wetness is critical for the growth of semi-insulating material from quartz crucibles. The Si concentration is suppressed by the use of wet  $B_2O_3$ , producing semi-insulating material; otherwise, with dry boric oxide the material becomes n-type. These studies indicate that the critical water content of the  $\mathrm{B}_2\mathrm{O}_3$ , above which semi-insulating GaAs is produced, is about 700-800 ppm. The specification of 700-800 ppm water in the  $B_2O_3$  can be met by commercial suppliers. However, at this and other laboratories, it has been observed that the incidence of twinning increases as the water content of the  $B_2O_3$  increases. This behavior is illustrated in Fig. 13. Therefore, it is difficult to meet the two basic requirements for device quality GaAs crystals using quartz crucibles - single crystallinity, which requires "dry" B203, and semi-insulating electrical properties, which require "wet"  $B_2 O_3$ . The use of PBN crucibles virtually eliminates Si contamination. Single crystal, twin-free semi-insulating material can be grown by using dry  $B_2O_3$  (also see Thomas et al., this volume, Section 5).

### 7. ELECTRICAL AND OPTICAL CHARACTERIZATION

An important question surrounding semi-insulating LEC GaAs has concerned the compensation mechanism by which the undoped material is semi-insulating. The understanding of the compensation mechanism has two important

practical consequences. First, knowledge of the cause-effect relationships between crystal growth and electrical characteristics of the material can greatly improve the yield of semi-insulating crystals in the growth process, as well as the crystal-to-crystal and wafer-to-wafer reproducibility. Second, this understanding can lead to improved device performance. For example, backgating effects may possibly be diminished by adjusting (Kocot and Stolte, 1981) trap levels in material intended for integrated circuit processing (see Stolte, this volume, Section 11).

Studies have shown that high resistivity material could be obtained when unintentionally doped material was exposed to oxygen (Haisty et al., 1962; Gooch et al., 1961). One explanation for this behavior was that a deep donor level associated with oxygen was responsible for the semi-insulating behavior. A deep level has been observed by photoconductivity (Lin et al., 1976) by optical absorption (Lin et al., 1976) and in transient capacitance experiments (Hasegawa and Majerfeld, 1975; Sakai and Ikoma, 1974) approximately 0.78 eV from the conduction band minimum and has been labeled EL2 or "O".

Transient capacitance (Kaminska et al., 1981), optical absorption (Lin et al., 1976) and photoconductivity (Lin et al., 1976) measurements indicate that the concentration of EL2 deep donors is not affected by the amount of  ${\rm Ga_2O_3}$  added to the melt or by the amount of oxygen in the material as determined by secondary ion mass spectrometry.

However, other studies indicate a different role for oxygen. There is evidence that oxygen can act as a getter for other impurities, such as silicon.

In this study, the effects of melt stoichiometry on the concentration of the deep donor EL2 and the effects of such changes on the electrical properties of the material have been studied. The results show that the stoichiometry of the melt controls the electrical compensation of the crystal through incorporation of EL2, a defect that has been implicated (Martin et al., 1980a) as the compensation-controlling center. These results indicate that (1) EL2 is the center responsible for the observed semi-insulating behavior, and (2) that EL2 is either an intrinsic defect or intrinsic defect complex.

Investigations in this study have included a number of techniques in an effort to determine which defects are important in affecting the compensation are the growth conditions under which these defects are produced. The LEC material was characterized through variable temperature Hall measurements, near infrared absorption, far infrared optical absorption, photoluminescence, photo-induced transient spectroscopy (PITS), and capacitance transient spectroscopy. The electrical characteristics of LEC GaAs crystals were evaluated by Hall effect measurements using samples obtained from the fronts and tails of the twelve crystals, and from detailed resistivity profiles of five crystals. The resistivity was found to be a strong function of the melt stoichiometry, as shown in Fig. 14.

Figure 14 shows that the material is semi-insulating (n-type) above, and p-type (low resistivity) below a critical As concentration in the melt of about 0.475 As atom fraction. The resistivity peaks at the critical composition at a value of about  $1.5 \times 10^8$   $\Omega$ -cm and decreases approximately 8 orders of magnitude below the critical composition. The resistivity also decreases very gradually as the As fraction increases from the critical composition.

The variation in resistivity across the melt composition range is explained in terms of the corresponding free carrier concentration and Hall mebility, as shown in Figs. 15 and 16. The semi-insulating material grown at the critical composition is n-type with a carrier concentration and mobility of  $1-2\times10^7$  cm<sup>-3</sup> and  $1-2\times10^3$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>m respectively. These Hall mobilities are low for n-type GaAs. As the As atom fraction increases from the critical composition to about 0.51, the mobility gradually increases to  $4-5\times10^3$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, which is more typical of n-type material. The corresponding electron concentration gradually increases to  $6-8\times10^7$  cm<sup>-3</sup>. The combined increase of both the mobility and carrier concentration leads to a reduction in resistivity of about one order of magnitude. The relatively low resistivity of the sample at 0.54 As fraction is due to an exceptionally low concentration of carbon.

The material becomes p-type below the critical composition. The free hole concentration rises approximately 9 orders of magnitude following a 1% reduction in As fraction in the melt from the critical composition. The hole concentration and Hall mobility of this material are in the range of  $1\text{--}3\times10^{16}~\text{cm}^{-3}$  and  $215\text{--}330~\text{cm}^2~\text{V}^{-1}~\text{s}^{-1}$ , respectively. Some of the mobilities obtained from the p-type material grown in the transition region, corresponding to melt compositions within about 1% of the critical composition, were very low, between 1 and 30 cm² V $^{-1}~\text{s}^{-1}$ . The measured hole concentrations were about 1  $\times$  10 $^{10}$  and 2  $\times$  10 $^{14}$  cm $^{-3}$ . These carrier concentrations are too high to explain the low mobilities in terms of mixed conduction. The low mobilities of material grown in the transition region could reflect inhomogeneities in the material. For instance, a striated pattern of regions of high and low resistivity could cause such behavior.

Detailed resistivity profiles of crystals grown from initially Asand Ga-rich melts further emphasize the role of the melt stoichiometry in controlling the electrical compensation as shown in Fig. 17. It is important to note that unless the initial melt is precisely stoichiometric (small differences between the stoichiometric and congruent melting compositions are neglected), As-rich (Ga-rich) melts become progressively more As-rich (Ga-rich) as the crystal is pulled from the melt. Crystals grown from As-rich melts were invariably semi-insulating from front to tail. Crystals grown from Ga-rich melts initially below the critical composition were p-type throughout. On the other hand, cryesals grown from Ga-rich melts initially above the critical composition underwent a transition from semi-insulating to p-type at the point along the crystal where the corresponding melt composition reached the critical value. This behavior clearly indicates that the resistivity is controlled by the melt stoichiometry, and that the semi-insulating to p-type transition is not related to the normal segregation of some common background impurity toward the tail of the crystal. Otherwise, the tail of As-rich-grown crystals would have become p-type as well.

Evaluation of the electrical and optical properties of the semi-insulating material indicates that the deep donor, commonly referred to as EL2, is the predominant deep center. An optical absorption band shown in Fig. 18 between 1 and 1.4  $\mu$ m previously identified with the EL2 center (Martin, 1981) was observed in all of the semi-insulating material. In addition, the activation energy of the electron concentration, obtained from plots of the temperature-corrected free electron concentration as a function of the reciprocal of temperature, was 0.75  $\pm$  0.02 eV. This energy is

tent with published values (Martin et al., 1980b) for the activation energy of EL2. The behavior of the photoconductivity thresholds (Lin et al., 1976) above and below 120K was also found to be consistent with the presence of EL2.

The concentration of EL2 in LEU GaAs samples was determined by optical absorption using the cross section reported by Martin et al., (1980b). Absorption due to unoccupied EL2 centers was not observed, and variable-temperature Hall measurements (300-420K) indicated that the centers were more than 90% occupied. Consequently, the absorption was taken to be proportional to the total EL2 concentration. The concentration of EL2 was found to depend on the melt stoichiometry, as shown in Fig. 19 increasing from about  $5 \times 10^{15}$  to  $1.7 \times 10^{16}$  cm<sup>-3</sup> as the As atom fraction increased from about 0.48 to 0.51. The concentration remained constant as the As fraction increased further to about 0.535.

The results of photoluminescence (PL) studies of the semi-insulating material are consistent with the measured dependence of EL2 on melt stoichiometry. Typical PL spectra at 4.2K of semi-insulating material grown from Asand Ga-rich melts, shown in Fig. 20 (curves a and b, respectively), exhibit bands peaking at 0.68 and 0.77 eV. The 0.68 eV band has been attributed (Yu et al., 1981) to radiative-recombination between EL2 electron traps and the valence band, and the 0.77 eV band to recombination possibly associated (Yu et al., 1981) with a hole trap. The intensity of the 0.68 eV band in the semi-insulating GaAs grown from Ga-rich melts (curve b) is substantially reduced by comparison with As-rich grown material (curve a). This behavior is consistent with the decrease of the EL2 concentration with decreasing As fraction (Fig. 19) as determined by optical absorption. Neither band was observed in the p-type material.

Photoluminescence spectra from p-type conducting material (Ga-rich), indicate the presence of an additional acceptor  $\sim$ 77 meV above the top of the valence band (Yu et al., 1981). Hall measurements show that this defect is the primary defect in the p-type undoped material.

The 77 meV acceptor was studied through infrared absorption. In Fig. 21, the room temperature (T = 300K) and low temperature (T  $\sim$ 20K) infrared absorbance spectra of unintentionally doped p-type GaAs are shown. Absorption at room temperature is due to two phonon lattice mode absorption (Cochran et al., 1961) and local vibrational mode absorption. In the low temperature spectra, three additional peaks are observed at energies 70.95 meV, 72.94 meV and 74.5 meV. These peaks are only observed below 50K in p-type material, indicating that the absorption is between different electronic states associated with an acceptor level. A comparison of spectra in these studies with previously published absorption and photoconductivity (Jones and Fisher, 1965; Kirkman et al., 1978) results for Ge and GaAs leads to the identification of these lines as transitions from the ground state to the  $2P_{5/2}(r_8)$ state (70.92 meV), the  $2P_{5/2}(r_7)$  state (72.95 meV), and a higher energy state (74.5 meV) which has previously been tentatively identified as the  $3P_{3/2}$ (Kirkman et al., 1978) state. Excellent agreement is obtained for the excited state splittings with this identification compared to those measured for other defects. Results for C, Zn, Si, and Mg (Kirkman et al., 1978) have given a value for the  $2P_{5/2}(r_7)-2P_{5/2}(r_8)$  splitting of 16 cm<sup>-1</sup> ± 1 cm<sup>-1</sup> compared to the value 16  $\pm$  0.5 cm<sup>-1</sup> obtained here. The splitting between the  $2P_{5/2}(\Gamma_8)$ and higher energy state has been reported as 28.8 cm<sup>-1</sup> compared to 28 cm $^{-1}$   $\pm$  1 cm $^{-1}$  observed here. As a result, the excited state structure can

be accurately described by effective mass theory for simple acceptors. The ground state energy can be estimated by setting the energy of the  $2P_{5/2}(r_8)$  state relative to the valence band at 7 meV. The value obtained, 78 meV, is consistent with theoretical values (~6 meV) and experimental estimates (76 meV) of this energy (Kirkman et al., 1978; Hunter and McGill, 1982) and is in good agreement with the value obtained from the luminescence measurements (77 meV).

By combining the results of Hall measurements with absorption measurements, the optical cross section of the transition to the  $2P_{5/2}(\Gamma_8)$  state was estimated to be  $\sigma_{opt}~\Delta E$  = 1.9  $\times~10^{-14}$  cm where  $\sigma_{opt}$  is the cross section and  $\Delta E$  is the full width at half maximum of the peak. The concentration of the 77 meV center in the crystals was determined from optical absorption using this cross section. The concentration of the center depends strongly on the melt stoichiometry, as shown in Fig. 22, for melt compositions above 0.47 As atom fraction, increasing from less than 1  $\times$  10  $^{15}$  cm $^{-3}$  to a level  $\sim$ 3  $\times$  10  $^{16}$  cm $^{-3}$  as the melt composition decreases from 0.47 to 0.43 As atom fraction. Local vibrational mode measurements and variable temperature Hall measurements indicate a background hole concentration of 3  $\times$  10  $^{15}$  -12  $\times$  10  $^{16}$  cm  $^{-3}$  from residual carbon acceptors. These acceptors prevent compensation of the 78 meV level in most cases. There is also some evidence that growth kinetics influence the incorporation of the defect. For example, capacitance-voltage profiles for implanted wafers along the length of a crystal indicate fluctuations in the trap concentration. These fluctuations affect the net carrier concentration near the crossover point from p-type material to semi-insulating material and contribute to the scatter in the data.

It is possible to rule out intrinsic defects which have symmetry lower than tetrahedral (TD). Such defects would have a split  $1S_{3/2}(\Gamma_8)$  ground state associated with the local strain field and short range impurity potential of the defect. In addition, the P states of the acceptor are mixed by such a field so that the  $2P_{5/2}(r_8)$  state would be split and the  $2P_{5/2}(r_7)$ state would be shifted in energy. The excellent agreement between these results and those obtained for substitutional impurities and the absence of additional splittings in these spectra indicates that such effects are small. The linewidth of the  $2P_{5/2}(r_8)$  state puts a limit on the magnitude of such a splitting at <5 cm $^{-1}$  (0.62 meV). Since the deformation potential associated with the ground state should be on the order of 1 eV, and because the acceptor wave function should be well localized on the defect, a much larger splitting would be expected for an axial or lower symmetry defect. For instance, the 150 meV Cu acceptor level is observed to have axial  $C_{3\,\text{V}}$  symmetry and has a different far-infrared spectra than the substitutional simple acceptor levels (Willman et al., 1973).

The defect responsible for the 78 meV level is most likely to be intrinsic in origin as opposed to an impurity related defect. The only impurity as determined by SIMS and LVM, occurring in these samples in sufficient concentration to be involved in this defect is boron. Although a  $B_{AS}$  defect would produce a double acceptor, no correlation was found between the boron content in the crystals and the concentration of the defect.

The 78 meV center is most likely associated with the antisite  $Ga_{As}$  or the arsenic vacancy. The levels associated with  $V_{As}$  are thought to lie somewhere near midgap (Bachelet et al., 1981). On the other hand, the first

ionization energy of the  $Ga_{As}$  acceptor is estimated to be very close to the value measured for this defect, 78 meV, by using simple scaling arguments.

Such an estimate is based on the point defect model for isocoric acceptors (Pantelides, 1978; Lipari and Baldereschi, 1978). Inspection of the Hamiltonian used by Baldereschi and Lipari for single acceptors shows that the energy is a function of the valence band parameters  $\mu$  and  $\delta$ , the effective spin-orbit splitting  $\overline{\Delta}$ , and the screening parameters  $A_i$  and  $B_i$ . The form of the Hamiltonian for the double acceptor levels of isocoric defects is similar and also depends only on these parameters. Values of these parameters are very similar in Ge and GaAs so an estimate of the  $Ga_{AS}$  levels can be made simply by scaling known values of the isocoric double acceptor Zn in Ge by the ratio of effective Rydbergs for the two materials. Using 32 meV for the first ionization of Zn in Ge, an energy of 84 meV is obtained for GaAs using Baldereschi and Lipari's estimates for the effective Rydbergs of the two materials.

This defect can also be compared to the well known native double acceptor in GaSb which is believed to be  ${\rm Ga_{Sb}}$  (van der Mulen, 1967). The theoretical basis for such a comparison is much weaker than in the previous case because  ${\rm Ga_{Sb}}$  is not isocoric and because the band parameters are considerably different in this case. Even so, good agreement is obtained with the Ge and GaAs values. Using an energy 34.5 meV for the native defect in GaSb (Noack et al., 1978) an energy of 83 meV is obtained for in GaAs.

If the 78 meV level is identified with the antisite  $Ga_{As}$ , it is possible to model the stoichiometric dependence of EL2 and the 78 meV level.

Although speculative, it is appealing to consider the identification of EL2 with the As antisite ( $As_{Ga}$ ) and the 78 meV level with the Ga antisite defects  $(Ga_{As})$ . Such an identification is supported by recent EPR measurements (Wagner  $\underline{\text{et al.}}$ , 1980) which indicate the presence of  $As_{Ga}$  in relatively large concentrations,  $10^{15}$ - $10^{16}~\mbox{cm}^{-3}$  in melt grown material. In addition, Van Vechten has predicted that such defects are potentially more stable than vacancy related defects and can be introduced by deviations from stoichiometry during growth (Van Vechten, 1975). Such an interpretation is consistent with these results. When the stoichiometry dependence of the 78 meV defect is compared to that of EL2, the concentrations of both defects extrapolate to zero at a melt composition near 0.47 As atom fraction. Such behavior can be explained by assuming that the  $As_{Ga}$  (EL2?) and  $Ga_{As}$  (78 meV) defects annihilate each other during the cool-down process by forming neutral antistructure  $As_{Ga}$ - $Ga_{As}$  defects. Since  $As_{Ga}$ - $Ga_{As}$  defects should have a relatively low enthalpy of formation (Van Vechten, 1975), these defects would presumably anneal out at relatively low temperatures. Thus, after cool-down only excess  ${\sf As_{Ga}}$  or  ${\sf Ga_{As}}$  defects remain, depending on whether the material was grown Asrich or Ga-rich. In such a case, the dominant defects in unintentionally doped melt grown GaAs would be either  $As_{\hbox{\scriptsize Ga}}$  or  $Ga_{\hbox{\scriptsize As}}$  depending on the stoichiometry of the melt.

Recent results in GaP support the antisite model (Kaufmann and Kennedy, 1981).  $P_{Ga}$  antisite defects in GaP have been found to occur in asgrown material. On the other hand,  $V_{Ga}$  defects have only been observed in electron irradiated material.

### 8. COMPENSATION MECHANISM

To develop a model for the electrical compensation in terms of the concentration of predominant electrically active centers in the semi-insulating material, the concentration of shallow and deep centers were related using simple theoretical considerations. The ionization of EL2 produces an ionized center plus an electron in the conduction band;

According to the principle of detailed balance, the concentration of ionized centers  $N_{\rm I}$ , the concentration of electrons n, and the concentration of unionized centers  $N_{\rm U}$ , are related by the following equation;

$$\frac{N_{I}n}{N_{II}} = K \qquad , \tag{2}$$

where K is a constant determined by the thermodynamics of the system.  $N_{\rm I}$  is equal to the net acceptor concentration, given as the difference in concentration between shallow acceptors,  $N_{\rm A}$ , and shallow donors,  $N_{\rm D}$ ;

$$N_{T} = N_{A} - N_{D} . (3)$$

the concentration of acceptors is given as the sum of the concentrations of carbon and other residual acceptors,  $N_A^R$ ;

$$N_{A} = [N_{A}^{carbon}] + N_{A}^{R} . \qquad (4)$$

The concentration of unionized centers is equal to the EL2 concentration as determined by optical absorption. That is, only EL2 centers which are occupied by electrons contribute to the optical absorption process;

$$N_{ij} = N_{Fi,2} \qquad . \tag{5}$$

By substituting Eqs. (3) through (5) into Eq. (2), the following expression for the free-electron concentration is obtained in terms of the predominant centers in the material:

$$n = K \frac{N_{EL2}}{([N_A^{carbon}] + N_A^R - N_D)}$$
 (6)

this expression can be rewritten in the following form:

$$[N_A^{carbon}] = K \frac{N_{EL2}}{n} + N_D - N_A^R . \qquad (7)$$

Therefore, the carbon concentration is proportional to the ratio of the EL2 concentration to the electron concentration.

The material was evaluated according to Eq. (7), measuring the carbon concentration (by LVM), the EL2 concentration (by optical absorption), and the electron concentration (by Hall effect measurements) for each sample. A plot of the carbon concentration as a function of the ratio of the EL2 concentration to the electron concentration, shown in Fig. 23, follows linear behavior,

indicating that the electron concentration is indeed controlled by the balance between EL2 and carbon. This result is independent of possible errors in the published values of the optical cross sections for carbon and EL2. It is important to note that if some other impurity were the predominant acceptor, such as Mn, Fe, Cu, Zn, or the 78 meV acceptor level, the linearity predicted on the basis of Eq. (7) would still necessarily hold. However, the linearity would not be distinguishable because the carbon term would be small compared to  $N_A^R$ ; the figure would be a scatter plot. In fact, the scatter in these data probably reflects actual fluctuations in the concentration of other background impurities rather than random error in the experimental measures. The small value of the intercept  $(N_D^-N_A^R)$  of the least-squares fit to the data also indicates the predominance of carbon acceptors. Thus, EL2 deep donors and carbon acceptors control the electrical compensation.

The variation of the electrical characteristics of the semi-insulating material (Figs. 14-16) with melt stoichiometry can now be explained on the basis of the analysis above. The EL2 concentration must either exactly match or exceed the carbon concentration to produce semi-insulating properties. The EL2 concentration in material grown from Ga-rich melts below the critical composition is insufficient to compensate the carbon, while in addition, the 78 meV acceptor appears leading to p-type conductivity. Semi-insulating material grown at the critical composition is closely compensated, leading to a maxima of the resistivity. As the As atom fraction in the melt increases from the critical composition to about 0.51, the EL2 concentration becomes progressively higher than the carbon concentration. As a result, thermal ionization of (unionized) EL2 centers (see Eq. (1)) gives rise to a gradual increase in

the electron concentration and a corresponding decrease in the resistivity (Figs. 15 and 14).

In practical terms, these results show that semi-insulating GaAs can be grown by the LEC technique reproducibly and with high yield provided that the melt is As-rich. This condition ensures that the melt will not become Garich during the growth process. The nine crystals grown during the course of this investigation from near-stoichiometric As-rich melts were semi-insulating from front to tail.

#### 9. RESIDUAL IMPURITIES

As discussed in the preceding section, the major electrically active centers in these LEC GaAs materials are deep donor EL2, the 78 meV acceptor (tentatively identified as Ga<sub>As</sub>) and the carbon acceptors. Using a technique known as photo-induced transient spectroscopy (PITS), the presence of other defect levels has also been detected. Although quantitative information regarding trap concentrations is not yet obtainable with PITS, the technique is useful in determining the presence of traps.

Photo-induced transient spectroscopy (PITS) is a transport technique which detects the transient rise or decay of the sample photocurrent during chopped illumination. A typical PITS spectrum is obtained by sampling either the photocurrent rise (R-PITS) or decay (D-PITS) at two points in time, with the difference  $\Delta I = [I(t_1)-I(t_2)]$  recorded continuously as a function of temperature. Any peaks observed in the spectrum will correspond to a trap emission rate  $e_t$  which is directly proportional to the sampling rate  $\Delta t^{-1} =$ 

 $(t_2-t_1)^{-1}$ . Successive temperature scans at different sampling rates can therefore determine both the trap energy and capture cross section, assuming a single-exponential rise or decay. In Table IX, a table of traps which have been observed using PITS is presented. Some of the more important of these are discussed below. Figure 24 shows a typical PITS spectra (note the logarithmic scale) comparing Cr and unintentionally doped LEC material. A major difference in the two spectra (outside of the Cr level) is the 0.52 eV hole trap.

The 0.52 ev hole trap (HL8) is due to Fe, and is particularly prevalent in Cr-doped samples, probably as a result of Fe contamination of the Cr. A second acceptor level at  $E_V$  + 0.35 eV has also been associated with Fe (Nakai et al., 1977) but only appears under conditions of light doping ( $\langle 5E15 \text{ cm}^{-3} \rangle$ ). A hole trap was observed at 0.34 eV,  $\sigma$  = 8E-14, but only in Bridgman and VPE material. The fact that this second level does not appear in the PITS spectra for undoped LEC material possibly indicates a lower degree of contamination in the LEC material.

The trap at 0.65 eV appears to be related to the pressure of oxygen in both Cr-doped and undoped material. It is particularly prevalent in LEC material grown from melts encapsulated by "wet"  $B_2O_3$  (Fairman et al., 1981) and its concentration is an effective end-point indicator for the suppression of Si incorporation from  $SiO_2$  crucibles.

This 0-related deep donor level was observed in both LEC and Bridgman material (Oliver et al., 1981) in concentrations estimated to be on the order of  $10^{15}$  or less. A hole trap at 0.83 eV,  $\sigma$  = 2E-13 (HL10) has also been

Table IX. TRAPS OBSERVED IN LEC GaAs FROM PITS

E <sub>T</sub> (eV) <sup>(1)</sup>	σ (cm <sup>2</sup> ) <sup>(2)</sup>	Identity <sup>(3)</sup>	Comments
0.15	8E-14 (n)	-	
0.18	8E-13 (u?)	-	*
0.14	1E-16 (n)	EL11	
0.26	2E-12 (u?)	-	# .
0.28	2E-12 (n?)	· ·	
0.30	4E-14 (p)	HL6	*
0.34	5E-14 (n)	EL6	*
0.26	1E-16 (n)	-	Si-O acceptor complex. 0.22 eV from dark conductivity
0.51	9E-13 (L.)	EL4	*
0.57	6E-13 (n)	EL3	*
0.52	1E-15 (p)	HL8	*Fe. Prominent within Cr-doping
0.65	8E-14 (n)	. · · · · · · · · · · · · · · · · · · ·	[0]-related. Also from dark conduct.
0.83	2E-13 (p)	HL10	
0.89	3E-14 (p)	HL1	*Cr acceptor
(0.74)	8E-14 (n)	EL2	*(From dark conductivity)

<sup>(1)</sup> Energy referred to 0°K bandgap, including energy (if any) associated with the cross section. (n) = donor level, (p) = acceptor level, (u?) - unknown.

<sup>(2)</sup> Cross section uncorrected for temperature dependence of the bandgap.

<sup>(3)</sup> From Martin et al., 1977.

All levels except 0.89 eV Cr acceptor appear in undoped material. \*Refers to Cr-doped material.

observed by PITS measurements, but curiously not simultaneously with the 0.65 eV level. This suggests that HL10 may be due to the 0-related level acting as a hole trap, but the large hole capture cross section would identify it as an acceptor level, inconsistent with the analysis of dark conductivity results. Furthermore, HL10 has prominently appeared in PITS spectra for LEC material grown with a "dry"  $B_2O_3$  encapsulant, in contrast with results for the 0.65 eV level. Therefore HL10 is tentatively assigned to a defect different from the 0-related level.

The electron trap at 0.57 eV (EL3) has appeared infrequently in LEC material, being far more prevalent in Bridgman growths. This level has been associated with point defects or point defect/impurity complexes (Itoh and Yani, 1980). The electron trap at 0.34 eV (EL6/EL7) occurs frequently in SI GaAs, including LEC material. It is prevalent in samples containing Fe or Cr, but not exclusively so.

A comparison of the defect levels occurring in Cr doped LEC, undoped LEC, and undoped Bridgman GaAs indicate a number of advantages for undoped LEC GaAs grown from PBN crucibles. By eliminating residual iron and silicon levels in the material, it is possible to reduce the number of defects in the material to a minimum. As a result, only the deep donor EL2, the 78 meV acceptor and the carbon acceptor are electrically significant in these LEC materials. The 78 meV acceptor concentration can be reduced by growing with the appropriate melt composition. In this way, semi-insulating material can be grown with high yield in a consistent fashion.

## V. LEC GaAs In Device Fabrication

Improvements in the quality of LEC semi-insulating GaAs dramatically affect the fabrication and performance of discrete microwave transistors and diodes, monolithic microwave integrated circuits and digital integrated circuits. This discussion, focusses on digital integrated circuits (ICs). The GaAs digital IC technology is presently undergoing rapid development with the aim of providing circuits that operate at higher switching speeds than is possible with silicon-based ICs (Eden et al., 1979; Van Tuyl et al., 1977; Mizutani et al., 1980). Most attention will be given to the technology developed at Rockwell International, as a representative example.

#### 10. APPROACH

Digital integrated circuits currently being developed are based on field-effect transistors. Most have Schottky-barrier gates (MESFETs), although structures with p-n junction gates (JFETs) or metal gates with intervening insulating layers (MISFETs) have also been reported (Zuleeg et al., 1978; Yokoyama et al., 1980). Additional circuit elements commonly include Schottky diodes and resistors of n-type GaAs (which may or may not be "saturated resistors," that is, 2 terminal devices which make use of the velocity - field characteristics of electrons in GaAs to achieve a desirable current-voltage nonlinearity). Typical circuit designs for digital gates are illustrated in Fig. 25. The circuits differ in the power consumed, levels of integration, and the requirements placed on the switching FETs. Figure 25(a) illustrates buffered FET logic (BFL), which was the first type of circuit design used with GaAs (Van Tuyl et al., 1977). Depletion mode (normally on)

FETs are used; relatively high power supply voltages, high pinchoff (threshold) voltages (>2 V), and high power consumptions have typically been employed to achieve gate propagation delay times below 100 ps. Figure 25(b) corresponds to Schottky-diode FET logic (SDFL). This design also makes use of depletion mode FETs, but allows a reduction in the power consumption at no cost in switching speed. Pinchoff voltages ~-1 V are typically used. The reduced power consumption permits a larger number of gates to be placed on the same chip. Operating circuits as shown in Fig. 26 containing more than 1000 gates have been reported with SDFL (Lee et al., 1980) and VLSI levels of integration appear feasible (>10,000 gates). The circuit of Fig. 25 (c) is direct-coupled FET logic (DCFL), which employs enhancement-mode (normally-off) FETs, and typically has the lowest power consumption requirements (Mizutani et al., 1980; Zuleeg et al., 1978). The logic voltage swings are lowest with this approach; they are limited by the Schottky barrier turn-on voltage to avoid conduction of substantial current from the gate to the source. The allowable variations in pinchoff voltage, processing, and substrate characteristics are also the smallest. Fabrication yield is currently a significant problem with this approach.

In addition to the three types of circuits referred to above, a variety of other circuit approaches and FET approaches have been demonstrated (Nuzillat, 1980). For all cases, however, at the high switching speeds achievable with GaAs, it is of major concern to maintain low-energy dissipation per switching operation, so that a high level of circuit integration can be obtained without excessive power dissipation per chip. The high level of integration is particularly advantageous because it reduces the system burden

of long-delay-time chip-to-chip interconnection, which might negate the system advantage obtained by using high speed gates. On the other hand, for low switching energy, logic swings, and voltage noise margins are reduced, placing stringent demands on the control over pinchoff voltage in the FETs. This requirement is further emphasized by the need for very high yield of FETs in order to produce circuits with large numbers of gates. The high degree of device reproducibility required for high system performance places stringent demands on the fabrication processes and substrate material characteristics.

Active regions for the FETs, diodes and resistors have been produced by epitaxial growth, by ion implantation, and by combinations of both (growth of an epitaxial "buffer" layer, followed by ion implantation). The most costeffective approach is that of ion implantation directly into semi-insulating substrates, which will be emphasized here. A typical fabrication sequence (Welch et al., 1980) is illustrated in Fig. 27. Polished wafers of (100) semi-insulating GaAs are coated with a thin (1000A) layer of Si<sub>3</sub>N<sub>4</sub> which protects the surface from mechanical and chemical damage during the process and serves as an annealing cap, as described below. Donor ions are implanted in the desired device areas, with the remaining regions of the sample protected by photoresist. The implanted ions are activated and the lattice damage from the implant is removed by a post-implant anneal. Subsequently, metallizations are deposited on the GaAs surface, in windows etched in the  $\mathrm{Si}_3\mathrm{N}_4$  cap. metallizations include, first, an ohmic contact layer typically of Au-Ge-Ni (which requires a subsequent alloy cycle), and a layer of Ti-Pt-Au, which serves both as Schottky gates and as first level of interconnects between devices. The metallizations are typically defined by a lift-off process;

metal linewidths in the Schottky gate region are typically 1 µm or less. To complete the circuits, a second level of interconnects is produced (in this case using Au) after appropriate deposition of an insulating layer of silicon nitride and via-hole opening (Lee et al., 1980).

The multiple, localized ion implant approach described above has a significant number of advantages over alternative techniques for producing the doped areas of the devices. The implantation technique is very flexible; a number of separate implants may be used, allowing independent optimization of the doping profile in different device regions. This capability is employed to obtain, for example, relatively heavily doped regions near the source and drain contacts to minimize series resistance in the switching FETs as well as to produce a low carrier density  $(8 \times 10^{16} \text{ cm}^{-3})$  thick (>3000A) active region for the Schottky diodes, to minimize diode capacitance. Isolation between devices is automatically obtained in the unimplanted areas through the semi-insulating substrate. The technique is cost effective since the throughput can be very high. Finally, the degree of control attainable in the doping concentration and thickness of the device areas is superior to most epitaxial techniques. A drawback of direct implantation is that the device characteristics are relatively sensitive to the substrate properties - a relationship which has motivated much of the recent research in LEC growth.

#### 11. SUBSTRATE INFLUENCE

The GaAs substrates can affect device performance in several ways. First, the doping concentration and distribution obtained for the donor implantation process can vary from ingot to ingot, and also from region to

region of the same ingot. Variations in electron mobilities in the doped regions may also occur. Second, the resistivity of unimplanted material has been found to decrease near the surface of wafers from a number of ingots during the post-implant anneal, which can cause a loss of invlation between devices. Third, the polished wafers typically must display good mechanical properties (size, flatness, parallelism, smoothness) in order to permit high quality optical lithography (needed for 1 µm long Schottky gates). Additional influences of the substrates on device performance have been suggested, but their existence has not been verified experimentally. These include effects of dislocations on current-voltage characteristics of devices, and effects of impurities or lattice imperfections on circuit reliability.

A typical implanted doping density profile for the FET channel region is shown in Fig. 28. These results were obtained from capacitance versus voltage measurements using Schottky barrier diodes produced on the sample surface. The peak carrier density is of the order of  $10^{17}$  cm<sup>-3</sup> and the depth is near 0.2  $\mu$ m, achieved with 400 keV, Se ions implanted into the GaAs with a fluence of typically 2.2  $\times$   $10^{12}$  cm<sup>-2</sup>. The ion energy is sufficient to penetrate the Si<sub>3</sub>N<sub>4</sub> cap layer that is deposited prior to the implantation. The doping density profile is approximately Gaussian in shape, although it has somewhat deeper tails than expected from a Gaussian dependence. The measured doping density in the tail region is affected by (a) a slight amount of channeling of the implanted ions (despite the fact that the ions are directed at the crystal 8° off the <100> orientation in order to minimize the channeling); (b) a slight amount of diffusion of the implanted Se during the 850°C post-implant anneal; and (c) the fact that the C-V technique used to get

the doping profile exhibits artifacts due to the proximity of the semiinsulating substrate.

From the circuit standpoint, one of the principal parameters of the implanted region is the pinchoff (threshold) voltage  $V_p$  measured in FETs or in Schottky diodes. The value of  $V_p$  corresponds to

$$V_{p} = \frac{q}{\epsilon} \int_{0}^{w_{s}} N_{d}(x) \times dx - V_{bi}$$
 (8)

where  $N_d$  is the net donor concentration in the implanted region (as discussed below), x is the distance from the surface,  $w_s$  is the effective depth of the profile,  $V_{bi}$  the built-in potential of the Schottky barrier, q the electronic charge and  $\varepsilon$  the static dielectric constant of GaAs. Variations in  $V_p$  occur principally as a result of changes in the doping distribution  $N_d(x)$  induced by variations in the substrate or in the implantation process. As discussed above, it is of interest for the fabrication of digital ICs to control  $V_p$  to within a relatively narrow range. For circuits of the SDFL type, control of  $V_p$  to within  $v_p$  to within  $v_p$  to within  $v_p$  to within  $v_p$  is the average pinchoff voltage of FETs in an area corresponding to an entire circuit.

The  $\langle V_p \rangle$  is affected by ingot-to-ingot and run-to-run reproducibility, as well as by long-range uniformity of the processed wafers. Too high a value of  $\langle V_p \rangle$  will result in FETs that will not turn off, while too low a value will lead to excessively slow circuit operation. An additional constraint is that of short-range uniformity of  $V_p$ , that is, the deviations of  $V_p$  from  $\langle V_p \rangle$  among the FETs of the same circuit must be small. This is necessary

to ensure that the input drive requirements of each gate will be met by the output capabilities of the preceding gates (after allowing for their fanout). The maximum tolerable standard deviation  $\sigma_{\rm V}$  of  $\rm V_p$  within a circuit is dependent on the circuit size; values of  $\sigma_{\rm V}$  of 50 mV appear to be needed for LSI circuits (>1000 gates).

To maintain the average pinchoff voltage  $V_p$  within the required  $\pm 200$  mV range, the maximum tolerable deviations in  $N_d$  are of the order of  $8 \times 10^{15}$  cm<sup>-3</sup>, assuming a uniform deviation over the 2000A thick channel. The maximum tolerable deviations in channel thickness are of the order of 80A. These tolerances are significantly more stringent than what is routinely achieved with epitaxial growth techniques.

The influence of the substrate on the measured  $V_p$  is principally through the net donor distribution  $N_d$ , as mentioned above. Here  $N_d$  is given by the expression

$$N_{d} = N_{implant} - N_{SA} - N_{DA} + N_{SD}$$
 (9)

where  $N_{implant}$  is the doping density introduced due to the implanted donors and  $N_{SA}$ ,  $N_{DA}$  and  $N_{SD}$  represent the substrate contributions of shallow acceptors, deep acceptors, and shallow donors, respectively, in the region of the implant.

The deep donors  $N_{\rm DD}$  do not influence the FET behavior since in the n-type channel region they are neutral. There is, however, an effect of the deep donors in producing slow shifts in FET characteristics when the channels

are nearly pinched off. As detailed earlier, it is typical of semi-insulating undoped LEC GaAs grown in PBN crucibles that there is a net excess of shallow acceptors over shallow donors. There are, in addition, more than enough deep donors to compensate out the net p-type shallow doping concentration. The deep acceptor concentration is typically small. Under these circumstances, it is expected that the net channel doping will be somewhat lower than the doping from the implant alone, in a variable amount depending on  $N_{\rm SA}$  -  $N_{\rm SD}$ .

This general behavior may be observed experimentally by making a series of donor implants into neighboring test wafers from the same ingot. Figure 29(a) shows, for example, the carrier density profiles obtained by implanting Si at 390 KeV with a series of fluences into a representative ingot. The carrier distributions scale approximately with fluence; however, if one plots the carrier density at a fixed depth (2500Å in this example) versus fluence, one obtained a linear relation that extrapolates back to a non-zero carrier density at zero fluence as shown in Fig. 29(b). For undoped LEC substrates grown from PBN crucibles this extrapolated value is typically negative (acceptor-like) with a value in the range 1 to 5  $\times$  10 $^{15}$  cm $^{-3}$ , in reasonably good agreement with the expected range of NSA - NSD on the basis of chemical analysis.

In contrast, Cr-doped Bridgman semi-insulating substrates display an extrapolated carrier density with a value in the range  $5-15\times 10^{15}~\rm cm^{-3}$ . This result corresponds to the fact that at the surface of the substrate there is an excess of shallow donors over shallow and deep acceptors while the substrate remains semi-insulating. In fact, this results from the phenomenon of Cr redistribution during the post-implant anneal. In the horizontal

Bridgman technique, typically, considerable amounts of Si contaminate the ingots due to decomposition of the quartz crystal growth apparatus at the growth temperature. With the silicon donors, the predominant shallow impurity, it is possible to obtain semi-insulating GaAs only by the intentional incorporation of deep acceptors (Cr) to pin the Fermi level near mid-gap. As part of the ion implantation process, however, a post-implant anneal (typically at 850°C) is needed to insure proper dopant activation. It has been shown by SIMS measurements that during this heat treatment considerable motion of the Cr typically occurs near the substrate surface.

Figure 30 shows, for example, the Cr profile obtained before and after an  $850^{\circ}\text{C}/30$  min anneal. The Cr is depleted over several microns from the surface. As a result, the silicon donor concentration may become undercompensated, yielding an n-type surface layer. If, however, the net donor concentration is small ( $<5 \times 10^{15}$  cm<sup>-3</sup>) and extends only over a thin layer, it is possible that the doped region will be completely depleted due to Fermi level pinning at the surface and in the bulk. In such a case, there will be no surface conductivity developed in the unimplanted material; only a slight donor-like contribution to the implanted channel will result.

The phenomenon described above is known as "thermal conversion" of horizontal Bridgman substrates - the formation of a conducting surface region on a previously high resistivity wafer as a result of heat treatment. Thermal conversion of wafers during integrated circuit fabrication gives rise to a loss of electrical isolation between devices, and consequent circuit failure.

A second type of thermal conversion has been identified, in which the surface of the wafer becomes p-type. This type of conversion is common when wafers are heated in a non-As containing ambient without an encapsulation layer, and is thought to be related to the pileup of Mn acceptors in the surface region. The incidence of p-type conversion, as well as of the abovementioned n-type conversion, depends on both the substrate material and the detailed processing. Possible processing variables include substrate cleaning techniques, chemical nature of the encapsulant, the deposition technique for the encapsulant, and anneal temperature and ambient.

Ingot selection techniques have been introduced at laboratories involved in fabricating integrated circuits, as a result of the variable incidence of thermal conversion among horizontal Bridgman ingots, as well as of the variable substrate donor contribution developed near the surface of the wafers. Samples slices from the front and tail of candidate ingots are submitted to qualification tests typically involving a test implant (to monitor the extra doping component contributed by the ingot, as well as to observe the mobility obtained) and a thermal treatment similar to the post-implant anneal (to see if any thermal conversion occurs). Experience at this laboratory showed that the fraction of ingots qualified from commercial suppliers of horizontal Bridgman ingots was ~30% or less. A dramatic change in qualification yield occurred with the introduction of LEC substrates. Virtually all the undoped ingots grown from PBN crucibles at Rockwell have passed the electrical qualification tests.

#### 12. IMPACT OF LEC GAAS

Introduction of the LEC material has also led to improved ingot-to-ingot reproducibility of pinchoff voltages in ion-implanted FET channel layers. The magnitude of the improvement in reproducibility is evident in the data of Fig. 31. Test chips were obtained from a variety of (qualified) horizontal Bridgman substrates and in-house-grown undoped LEC substrates; the test chips were processed together, capped with  $\mathrm{Si}_3\mathrm{N}_4$ , implanted with Se, annealed, and the resultant effective pinch-off voltage  $\mathrm{V}_p$  determined with the C-V technique. In this fashion, variations in the results due to process-induced effects were minimized. A standard deviation of 304 mV is displayed among the Horizontal Bridgman samples, even after excluding 2 of the 12 ingots which in fact displayed unqualified behavior (due, presumably, to nonuniformity within the previously-tested ingot). The distribution of  $\mathrm{V}_p$  among the 9 undoped LEC ingots grown from PBN crucibles is significantly tighter; the corresponding standard deviation was 95 mV.

The radial and longitudinal uniformity of the ingots has been another important advantage of the LEC-grown substrates over the horizontal Bridgman material for digital ICs. The growth size and geometry, and the absence of Cr, decrease the effects of impurity segregation in the LEC material. As a result, pinchoff-voltages of FETs tend to display smaller variations across fabricated wafers when LEC substrates are used. The uniformity of FET characteristics has been studied at Rockwell for a number of years. To facilitate the study, an array of 1 µm gate length test transistors is included on each processed wafer, and after completion, an automated test setup is used to probe the devices and accumulate the corresponding statistics and wafer maps

(Zucca et al., 1980). Figure 32 indicates the degree of uniformity in threshold voltage distribution possible with undoped LEC GaAs; a standard deviation of 25 mV is measured for these transistors, distributed across the IC wafer, which measures 25 mm  $\times$  25 mm on a side (and is thus smaller than a typical slice from an ingot).

To compare the uniformity of HB and LEC substrates, it is of interest to compare the  $\rm V_p$  statistics for a number of wafers. Over a 6-month period, for example, in which more than 50 wafers (including both HB and LEC material) were processed, the median standard deviation of  $\rm V_p$  across the wafer was 85 mV for the Bridgman material, and 55 mV for the LEC material. It should be noted that the pinchoff voltages of FETs close to one another on a wafer are correlated, so that the standard deviation of  $\rm V_p$  within a relatively small neighborhood (with dimensions on the order of milimeters) is smaller than that obtained over the entire wafer. No significant differences have been noted between the short range statistics for Horizontal Bridgman and LEC material. The low amount of variation obtained in both cases is favorable for the high-yield fabrication of LSI circuits.

To further probe the uniformity of LEC substrates, Se implants have been carried out on wafer sections larger than the IC wafers used to date at this facility. Figure 33 shows, for example, a map of effective pinchoff voltage as obtained from C-V measurements on a quarter of a 3-inch LEC wafer. The standard deviation of  $V_p$  is only 39 mV (2.8% of the mean). Additional data are shown in Fig. 34, which indicates the high degree of uniformity of  $V_p$  obtained among test chips selected along the length of an LEC ingot.

The size and shape of LEC substrate material should have a major long-term impact on the fabrication procedures for GaAs ICs. At this laboratory, a fabrication line is in place employing 3-inch diameter round (100) GaAs wafers. Considerable economy results from using photolithography, plasma-etching, metal deposition, and other equipment designed and optimized for silicon wafer processing. At the same time, the expanded area per wafer should contribute to the reduction of processed GaAs chip costs.

There has been concern regarding the effect of dislocations in LEC GaAs on device performance and reliability. Preliminary studies indicate that the performance of ICs is not affected by substrate dislocations. For example, some of the larger integrated circuits fabricated at in this facility have been produced on substrates with  $2\times10^5$  cm<sup>-2</sup> dislocation density. These circuits contain sufficient FETs and diodes that the probability is close to unity that at least one FET channel region or Schottky diode active region is traversed by a dislocation. The successful operation of the circuits with reasonable yield indicates that a single dislocation is not a fatal flaw.

In summary, undoped LEC GaAs substrates have had a positive impact on the fabrication of digital ICs. The uniformity and ingot-to-ingot reproducibility of implanted FET channel characteristics have been markedly improved, and the problem of thermal conversion has been eliminated, making the ingot qualification procedures formerly employed no longer critical. The availability of material has improved considerably, and the size and shape of the wafers are conducive to batch fabrication with available semiconductor processing equipment. At the same time, there appear to be no detrimental effects from the higher dislocation density generally associated with LEC material.

### VI. Conclusions

These investigations of undoped, semi-insulating LEC GaAs have focused on four principal issues; the crystal growth technology, structural perfection, electrical properties, and the behavior of the material during device processing. The results have brought about a considerable improvement in the understanding of the cause-effect relationships between properties of the material and crystal growth parameters. Through these results, undoped, semi-insulating material can be grown reproducibly with good yield primarily through proper control of the stoichiometry. Furthermore the undoped LEC material has demonstrated the uniform, thermally stable properties required for GaAs device fabrication. The LEC GaAs material offers superior properties for device fabrication and control of device parameters, particularly depletion-mode digital integrated circuits.

#### 13. ELECTRICAL PROPERTIES AND COMPENSATION MECHANISM

The key to the reproducible growth of undoped semi-insulating GaAs by the liquid encapsulated Czochralski technique is the control over the melt stoichiometry. Evidence presented indicates the free carrier concentration is controlled by the balance between EL2 deep donors and carbon acceptors; furthermore, the incorporation of EL2 is controlled by the melt stoichiometry, increasing as the As atom fraction in the melt increases. As a result, semi-insulating material can be grown only from melts above a critical As composition. Using the <u>in situ</u> synthesis, As can escape from the charge during the heat-up cycle through sublimination with the loss of significant quantities of As. Ga-rich melts and p-type (low resistivity) crystals can

result from this loss, which depends on at least two parameters, the crucible material, and the initial heating rate of the charge.

The empirically-determined dependence of the concentration of EL2 (and the 77 meV acceptor) on melt stoichiometry provides strong evidence for the existence of electrically active native defects in GaAs. Although it is generally acknowledged that native defects could play an important role in controlling the properties of GaAs, no consistent picture has yet emerged concerning the nature and properties of the defects. However, results from these studies show that native defects can have profound effects on the electrical characteristics of bulk material. The connection between EL2 and a native-defect in bulk LEC GaAs is consistent with published work on GaAs grown by vapor phase epitaxy and organometallic chemical vapor deposition. These previous reports showed that the EL2 concentration increases as the As-to-Ga ratio in the vapor increases. Isolated native defects which would follow the observed stoichiometry dependence of EL2 include the gallium vacancy  $V_{\rm Ga}$ , the arsenic interstitial As; and the arsenic-on-gallium antisite,  $\mathsf{As}_\mathsf{Ga}\text{-}$  Since  $\mathsf{V}_\mathsf{Ga}$ would be expected to be an acceptor, EL2 would more likely be related to one of the latter two defects.

A second stoichiometry-related defect, an acceptor, found in material grown from Ga-rich melts was also identified. Interpretation of the optical absorption spectra and variable-temperature Hall measurements suggests that the center is a gallium-on-arsenic antisite ( $\text{Ga}_{As}$ ) double acceptor. The defect is complementary to EL2: the concentration of both defects is about  $5 \times 10^{15}$  cm<sup>-3</sup> in material grown from melts with a concentration of 0.47-0.48 As atom fraction; the EL2 concentration in the material increases above this

As composition in the melt, while the acceptor concentration increases below this melt composition. The complementary nature of these defects would suggest that EL2 is an arsenic-on-gallium antisite  ${\sf As}_{\sf Ga}$ .

An issue yet to be resolved concerns the thermal annealing behavior of native defects, during both crystal growth and device processing. The solidification process takes place at the melting point of GaAs (1238°C), or a few degrees below this temperature, depending on the degree of non-stoichiometry in the melt. The material remains at elevated temperatures for several hours after solidification, cooling slowly as the crystal is pulled from the melt, and the growth chamber is slowly brought to room temperature. It is highly likely that the "grown-in" defect density undergoes some change in concentration during this cooling process.

#### 14. STRUCTURAL PERFECTION

The density and distribution of dislocations in 3" diameter, undoped GaAs crystals grown by the liquid encapsulated Czochralski technique have been characterized. The radial distribution across wafers exhibits a "W"-shaped profile indicating excessive thermal gradient-induced stress as the primary cause of dislocations. The density along the body of each crystal increases continuously from front to tail. In contrast, the longitudinal distribution in the cone region is inverted, first increasing, and then decreasing as the crystal expands from the neck to full diameter. Growth parameters favoring reduced dislocation densities include good diameter control, and the use of thick  $B_2O_3$  encapsulating layers, slightly As-rich melts, and low ambient pressures. The dislocation density in the body of the crystal is practically

independent of cone angle  $\theta$  for 20°< $\theta$ <70°. However, high densities result for flat-top (0°< $\theta$ <20°) crystals. Dash-type seed necking reduces the dislocation density only when high density seeds (>5000 cm<sup>-2</sup>) are used. Further, studies revealed that convective heat transfer from the crystal to the high pressure ambient plays a dominant role in controlling the dislocation density.

Low-dislocation, 3" diameter GaAs can be grown by the LEC technique. Material has been produced at this laboratory with EPDs as low as  $6000~\rm cm^{-2}$  in selected regions of the crystal. The average EPD over approximately 80% of the area of 3" diameter wafers has been less than  $5\times10^4~\rm cm^{-2}$ . Further reductions in dislocation density are expected through proper control of the crystal growth parameters, including, for example, the use of thick  $B_2O_3$  encapsulating layers to reduce the radial gradients, and reduction of the growth pressure to decrease the heat transfer at the crystal ambient surface, (provided that the thermal degradation of the crystal can be controlled). Modification of the crystal growth configuration to reduce convective heat transport in the ambient would also be beneficial.

#### 15. CRYSTAL GROWTH TECHNOLOGY

Advances made in diameter control and in reducing the incidence of twinning are important recent accomplishments in the LEC crystal growth technology. Since single crystalline wafers with the (100) orientation are required for integrated circuit application; twin formation during crystal growth (leading to changes in crystallographic orientation) and polycrystallinity, must be avoided. Studies indicate that one of the most important growth parameters for the control of twinning is the melt stoichiometry - the

incidence of twinning is significantly reduced when crystals are grown from As-rich melts. A yield of single crystalline material of over 90% has been achieved by growing from As-rich melts, with further improvements expected with tighter control over the melt stoichiometry.

The success and cost-effectiveness of GaAs device technology will ultimately depend on the availability of round, uniform-diameter wafers for automated device fabrication. The first step in achieving this is the growth of crystals with a uniform diameter (also shown to be important in maintaining a low dislocation density). Through proper control of the growth parameters (i.e., cooling rate, crystal rotation and pull rate, and crucible rotation and lift rate) the diameter can be controlled manually to a tolerance as low as  $\pm 1.1$  millimeters and with a routine tolerance of better than  $\pm 3$  millimeters. This degree of diameter control together with centerless grinding, results in the maximum yield of usable material. Although further reductions in the dislocation density will accompany reductions in the radial temperature gradients in the growth system, the lower gradients will likely lead to increased difficulties in maintaining diameter control. Therefore, automatic diameter control will eventually become necessary for the production of large-diameter material for integrated circuit applications.

#### 16. APPLICATION TO ICS

The progress achieved through these studies of the LEC growth technique for undoped semi-insulating GaAs has resulted in substantial improvements in the uniformity and reproducibility of critical parameters of integrated circuits. The electrical and crystalline parameters exhibited by

these materials are superior to those observed from materials grown by other techniques, and meet the requirements for use in the fabrication of LSI devices.

#### **ACKNOWLEDGEMENT**

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#### FIGURE CAPTIONS

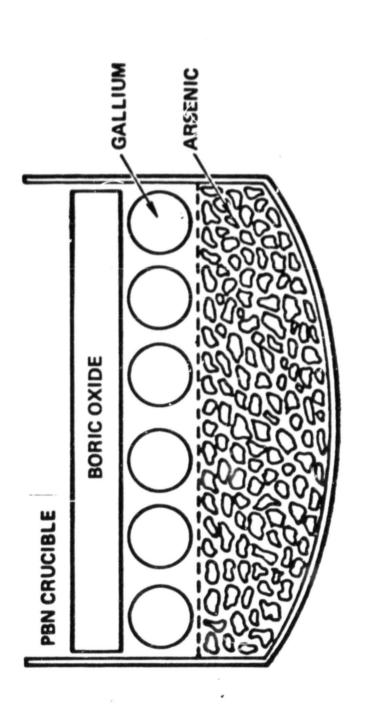
- Fig. 1 Cross section of the LEC crucible before growth showing the charge of elemental Ga and As and the preformed  $B_2O_3$  disc.
- Fig. 2 Cross section of the crucible for the LEC growth system, showing the location of the  ${\rm B}_2{\rm O}_3$  during growth.
- Fig. 3 Cross section of the LEC system during growth with a Si<sub>3</sub>N<sub>4</sub> coracle.
- Fig. 4 Photograph showing the neck, cone, and full-diameter sections of an LEC crystal.
- Fig. 5 Slicing diagram for (100) GaAs crystal. (From Chen et al., 1983.)
- Fig. 6 Photograph of KOH-etched, 3 in. (100) LEC GaAs wafer showing fourfold symmetry, (showing (1) ring, (2) center, and (3) edge regions. (From Holmes et al., 1983.)
- Fig. 7 Photomicrographs of regions on a KOH-etched (100) LEC GaAs wafer cut from the front of ingot No. 18/M, showing radial distribution of dislocations on three-in. diameter wafer, and (1) ring, (2) center, and (3) edge regions. (From Chen et al., 1983.)
- Fig. 8 Radial and longitudinal dislocation density for 3-inch LEC GaAs crystal. (From Chen et al., 1983.)
- Fig. 9 Dislocation maps of longitudinal cross sections of ingot cones grown with varying cone angles. (From Chen et al., 1983.)
- Fig. 10 Dislocation maps of longitudinal cross sections of seeds, necks, and tops of cones with varying neck diameters: (a) 1.6 mm neck diameter showing severe deformation in the neck region, (b) 3 mm neck diameter showing dramatic dislocation density reduction. (From Chen et al., 1983).)

- Fig. 11 Bright field micrograph for: (a) an As-rich sample (No. 11T)  $\frac{1}{9}$  = <02 $\frac{1}{2}$  > s = 0, foil thickness ~750Å, 73,000 X. (b) LEC GaAs sample (No. 8T) g = <02 $\frac{1}{2}$  >, s = 0, foil thickness ~750Å, 120,000 X.
- Fig. 13 Dependence of Si and B concentrations and twinning in LEC GaAs on water content of  $B_2O_3$  encapsulant. Numerals near data points indicate number of crystals used to ascertain average value.
- Fig. 14 Dependence of electrical resistivity of LEC GaAs on melt stoichiometry. Semi-insulating material is obtained above, and p-type (low resistivity) material below a critical melt composition of about 0.475 As atom fraction. (From Holmes et al., 1082a.)
- Fig. 15 Dependence of free carrier concentration of LEC GaAs on melt stoichiometry. The semi-insulating material is n-type, and the free electron concentration increases gradually as the As concentration in the melt increases from the critical composition. The free carrier concentration rises approximately 9 orders of magnitude following a 1% reduction in As fraction from the critical composition. (From Holmes et al., 1982b.)

- Fig. 16 Dependence of Hall mobility of LEC GaAs on melt stoichiometry. The mobility of the semi-insulating material varies from  $1\text{-}2\times10^3$  to  $4\text{-}5\times10^3$  cm $^2$  V $^{-1}$  s $^{-1}$  as the As atom fraction increases from the critical composition to about 0.535. The mobility of the p-type material grown in the transition region, within about 1% of the critical composition, is low, between 1-30 cm $^2$  V $^{-1}$  s $^{-1}$ . The mobility of the p-type material grown outside of the transition region ranges from 215 to 330 cm $^2$  V $^{-1}$  s $^{-1}$ . (From Holmes et al., 1982b.)
- Fig. 17 Resistivity profiles for LEC GaAs crystals grown from Ga-rich and As-rich melts. (From Holmes et al., 1982a.)
- Fig. 18 Optical absorption of the deep donor EL2 in semi-insulating LEC GaAs.
- Fig. 19 Dependence of EL2 concentration as determined by optical absorption on the melt stoichiometry. The concentration of EL2 increases from  $5 \times 10^{15}$  cm<sup>-3</sup> to  $1.7 \times 10^{16}$  cm<sup>-3</sup> as the As atom fraction increases from about 0.48 to 0.51, and appears to saturate as the As concentration increases further to 0.53. (From Holmes et al., 1982a.)
- Fig. 20. Typical photoluminescence spectra of semi-insulating GaAs grown from (a) an As-rich melt (As atom fraction 0.507,  $\rho$  = 1.8 × 10<sup>7</sup>  $\Omega$ -cm) and (b) a Ga-rich melt (As atom fraction = 0.488,  $\rho$  = 1.4 × 10<sup>8</sup>  $\Omega$ -cm). The intensity of the 0.68 eV band decreases as the As atom fraction decreases toward the critical composition consistent with the optical absorption measurements (Fig. 18). (From Holmes et al., 1982b).

- Fig. 21. Far infrared absorption spectra of 78 meV acceptor in GaAs. At room temperature only phonon absorption is observed. At lower temperatures the spectrum associated with the acceptor is observed. (From Elliott et al., 1982.)
- Fig. 22. Stoichiometry dependence of the 78 meV acceptor. The concentration of the 78 meV acceptor increases rapidly from 0.47 As atom fraction to approximately  $3 \times 10^{16}$  cm<sup>-3</sup> at 0.43 As atom fraction. (From Elliott et al., 1982.)
- Fig. 23 Dependence of the carbon concentration on the ratio of the EL2 concentration to the electron concentration. The concentration of carbon, EL2, and electrons was determined for each sample. The dashed line is a least-square fit to the data. The linearity of the data indicates the dominant roles played by EL2 deep donors and carbon acceptors in controlling the compensation (see text). The small value of the intercept  $(N_D N_A^R)$  also indicates the predominance of carbon acceptor. (From Holmes et al., 1982b.)
- Fig. 24 Normalized photo-induced transient spectroscopy data for chromium doped LEC (3F) and Bridgman (39210F) GaAs.
- Fig. 25 Circuit diagrams for three GaAs logic approaches: (a) buffered FET logic; (b) Schottky diode FET logic; (c) direct coupled FET logic.
- Fig. 26 Photograph of  $8 \times 8$  multiplier fabricated on LEC GaAs. The circuit contains 1008 gates.
- Fig. 27 Fabrication steps for planar fabrication process using localized implantation into semi-insulating GaAs. Note that the bare surface of the GaAs is never exposed, except for the areas where the encapsulating dielectric is briefly open for metal depositions.

- Fig. 28 Carrier concentration profiles for ion implanted FET channel-type regions in semi-insulating GaAs, showing the difference in profile shape between substrates which are thermally stable and those which undergo surface conversion.
- Fig. 29 (a) Carrier concentration profiles for various fluences of Si implants into semi-insulating GaAs. (b) Plot of carrier concentration (at 0.25 μm depth) vs. Si fluence for implants into three different substrates. The intercept at zero fluence is an indication of the substrate contribution to the doping. Ingot G17-27I was grown by the Bridgman method, the other two ingots were grown by the LEC method.
- Fig. 30 SIMS data indicating the Cr concentration profile in annealed and unannealed Cr-doped GaAs.
- Fig. 31 Histograms comparing the variations in pinchoff voltage among different ingots of undoped LEC and Bridgman GaAs.
- Fig. 32 Histogram showing the variation in pinchoff voltage across a 1 in. processed wafer of undoped LEC GaAs, showing minimal variations.
- Fig. 33 Map of a quarter of a 3-in. LEC undoped LEC wafer showing variations in the depletion voltage across the length of an undoped LEC ingot.
- Fig. 34 Variation of depletion voltage along the length of an undoped LEC ingot.



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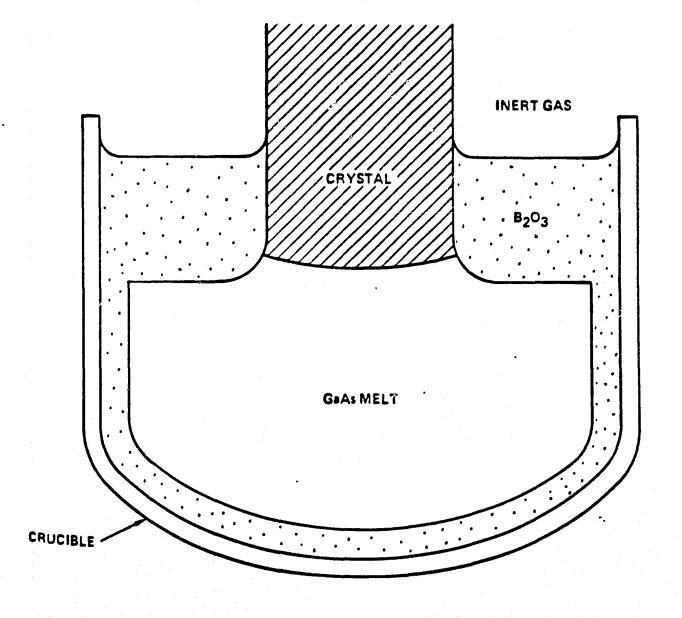


Figure 2

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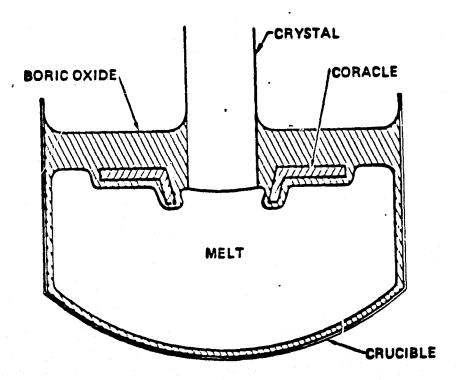


Figure 3

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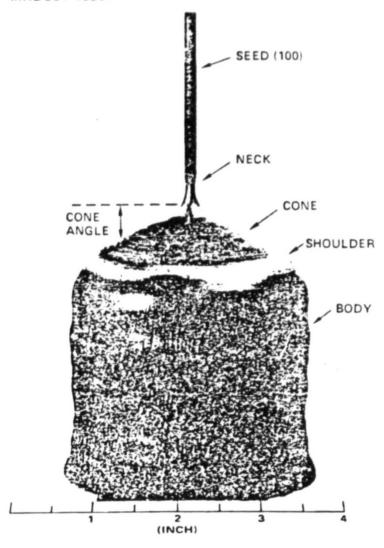


Figure 4

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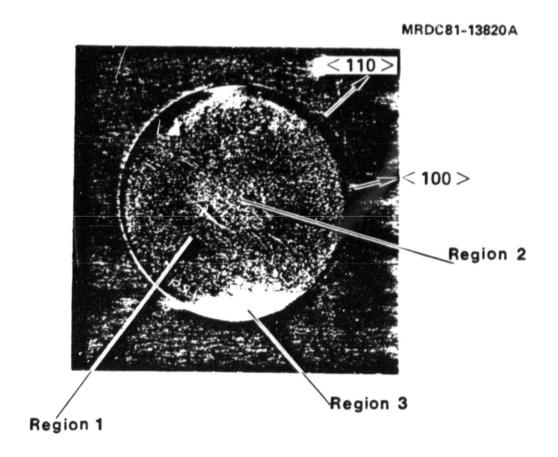


Figure 6

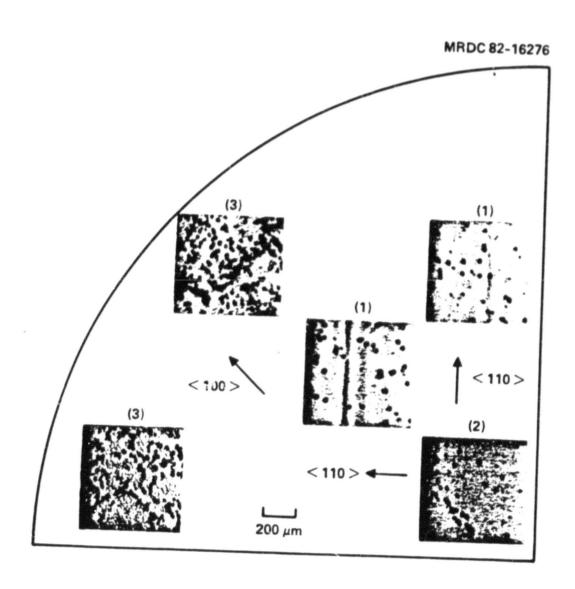


Figure 7

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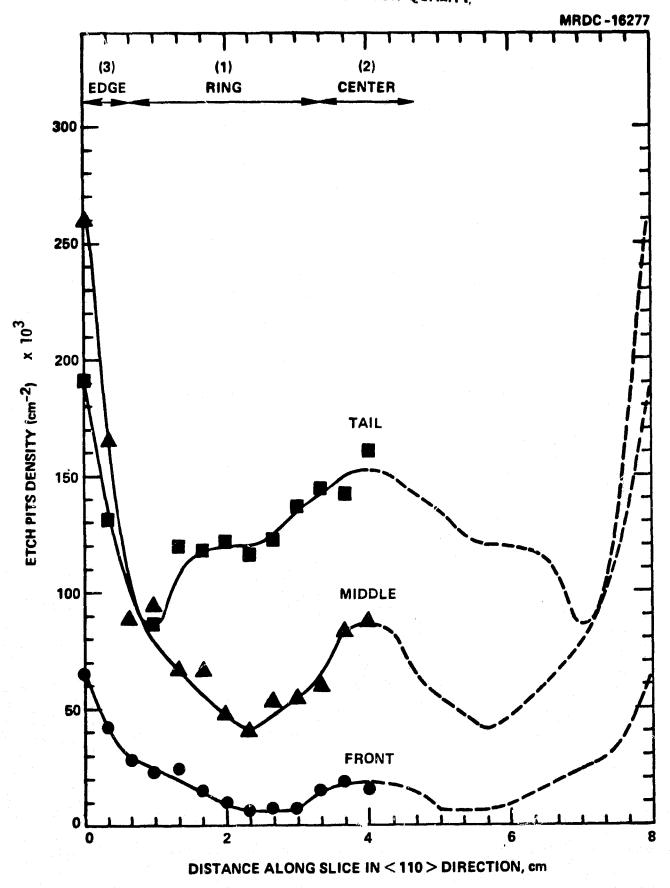


Figure 8

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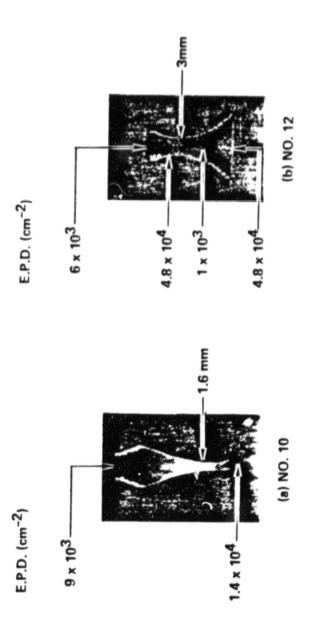
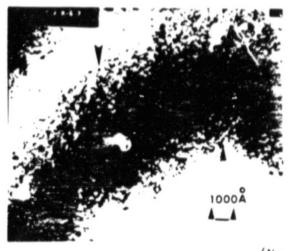


Figure 10

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#### MRDC81-13822



a) B.F. MICROGRAPH FOR AN As-RICH SAMPLE (No. 11T)  $\overline{g} = \langle 02\overline{2} \rangle$ , s = 0, FOIL THICKNESS ~ 750 Å, 73,000 X.

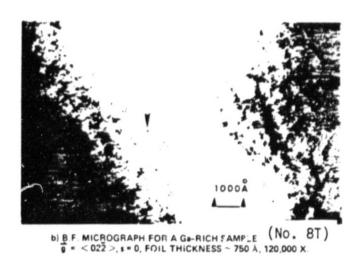
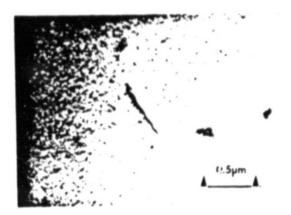


Figure 11

#### MRDC81-13823



a) B.F. MICROGRAPH FOR A TYPICAL LEC GaAs SAMPLE.  $\hat{g} = < 0\bar{2}2 >$  , s > 0, 38,090 X.



b) B.F. MICROGRAPH FOR AN As-RICH SAMPLE  $\hat{g} = \langle 0\bar{2}2 \rangle$ , s > 0, 13,000 X.

(No. 11T)

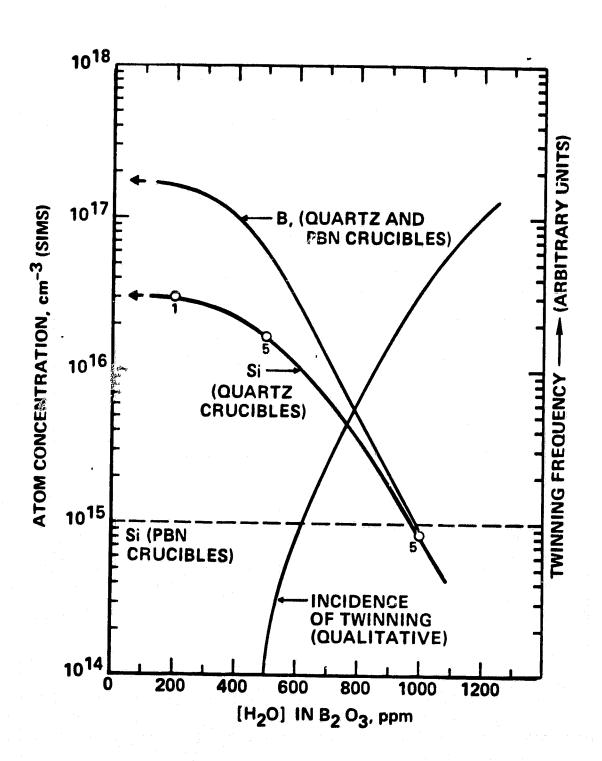
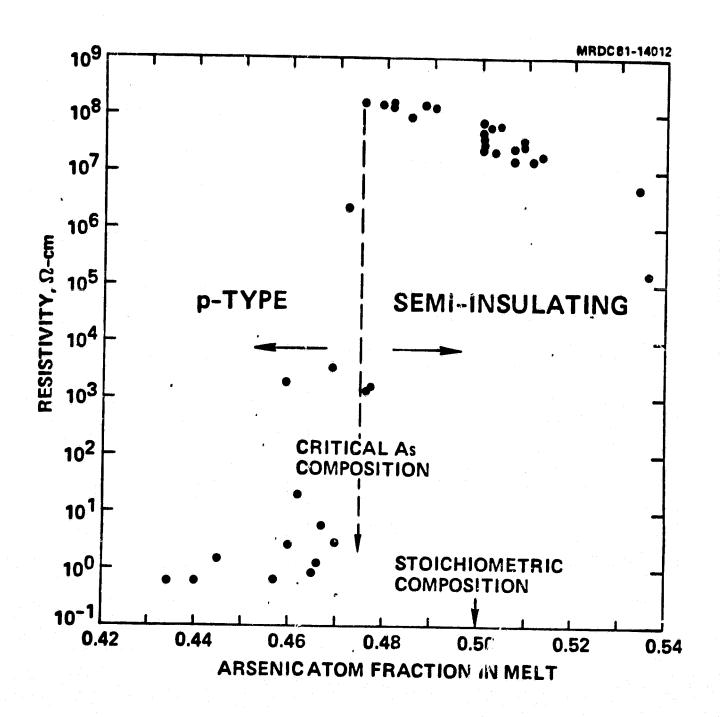


Figure 13



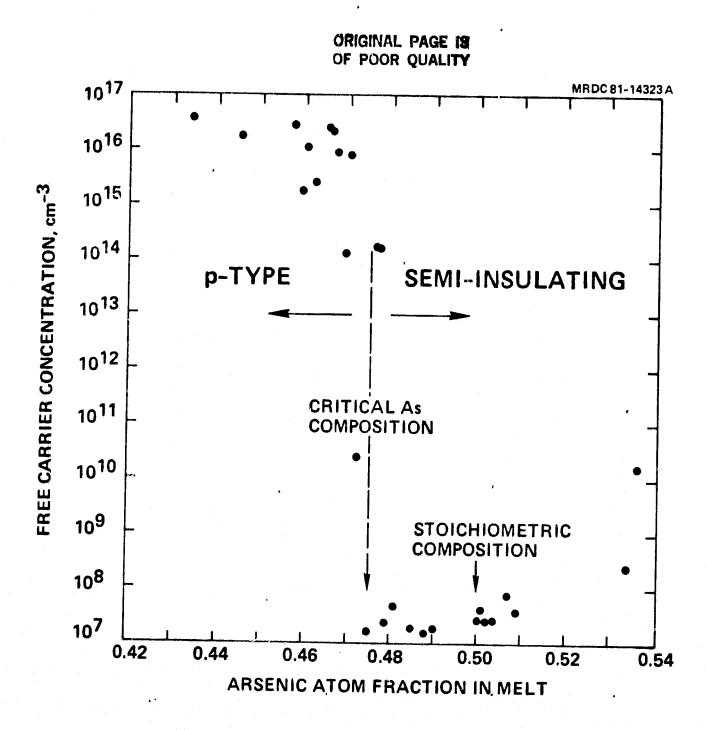
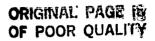


Figure 15



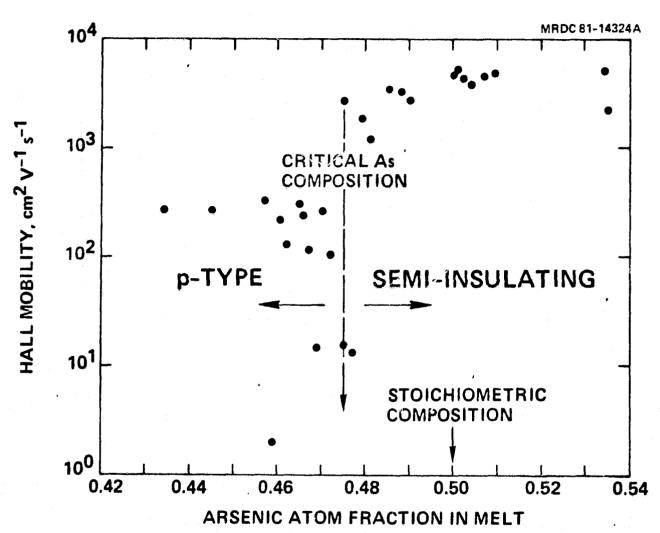


Figure 16

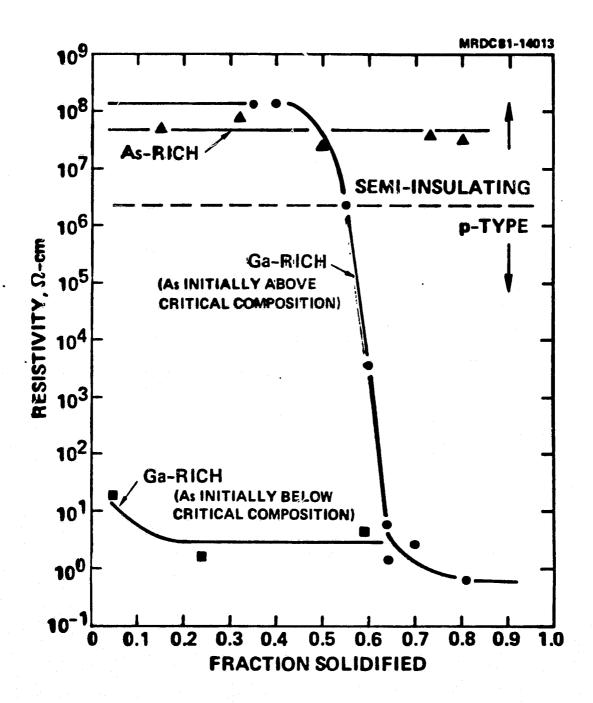


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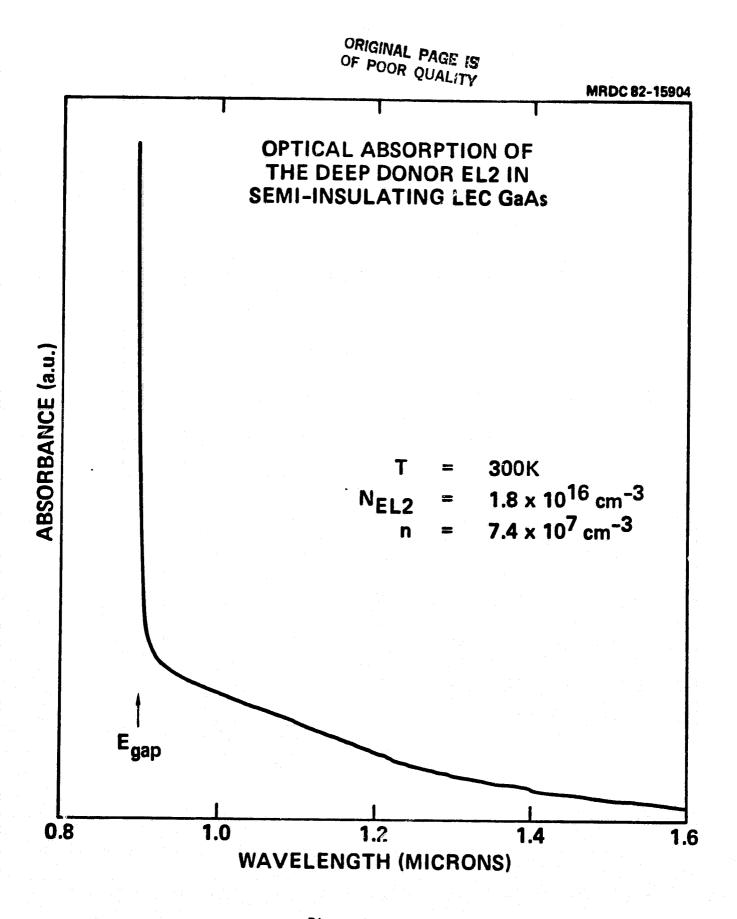
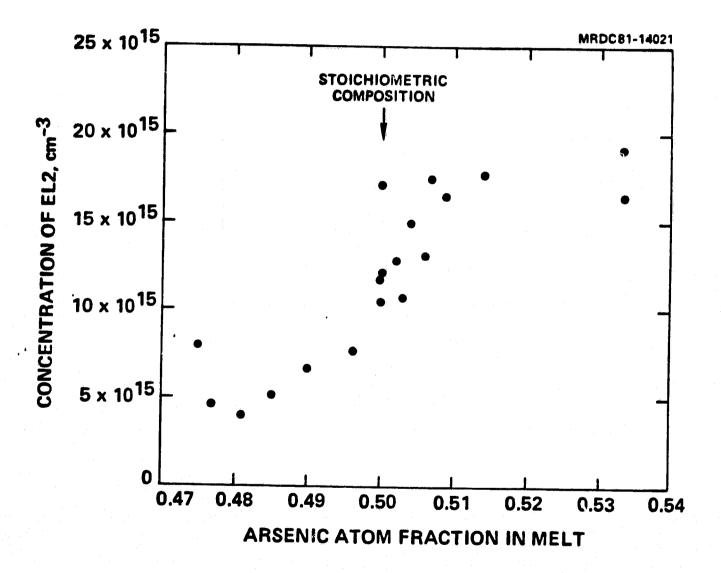


Figure 18

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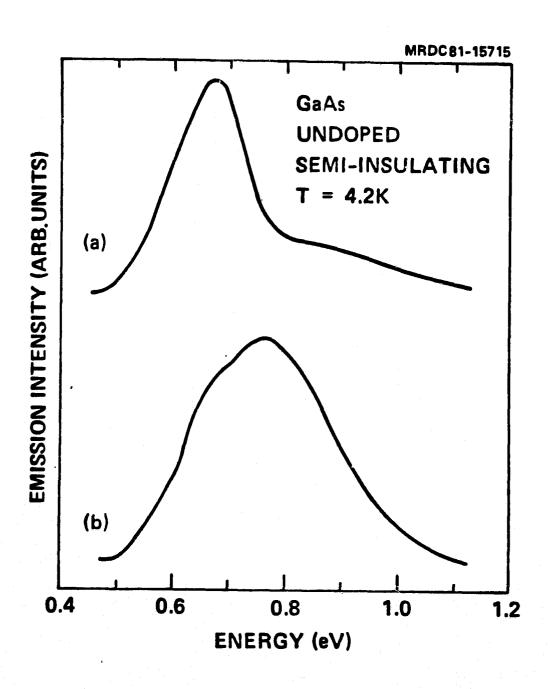


Figure 20

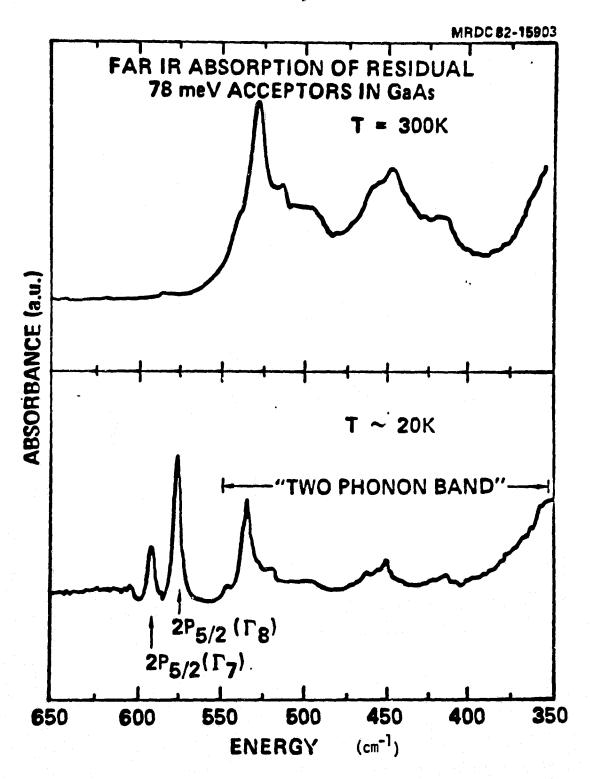


Figure 21

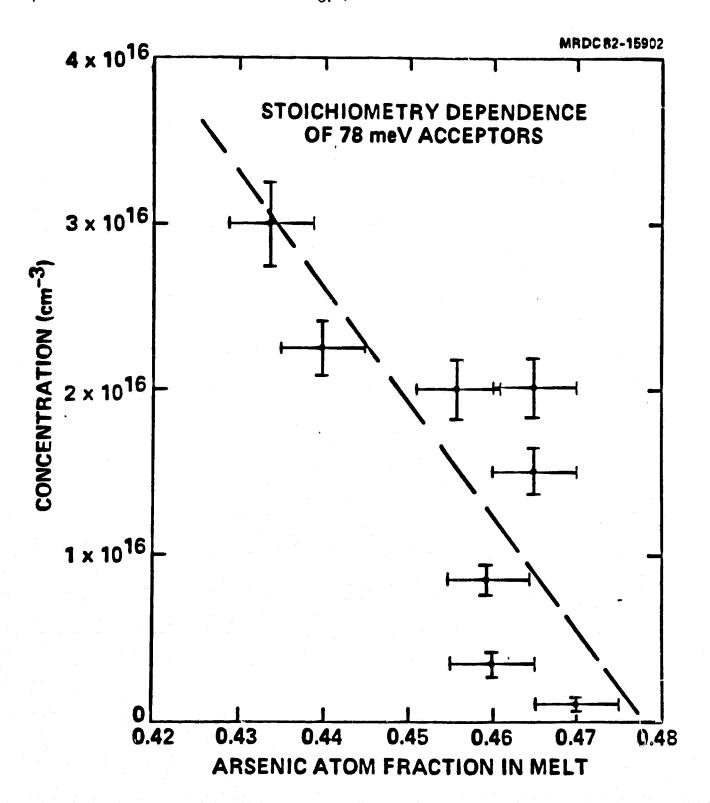
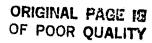


Figure 22

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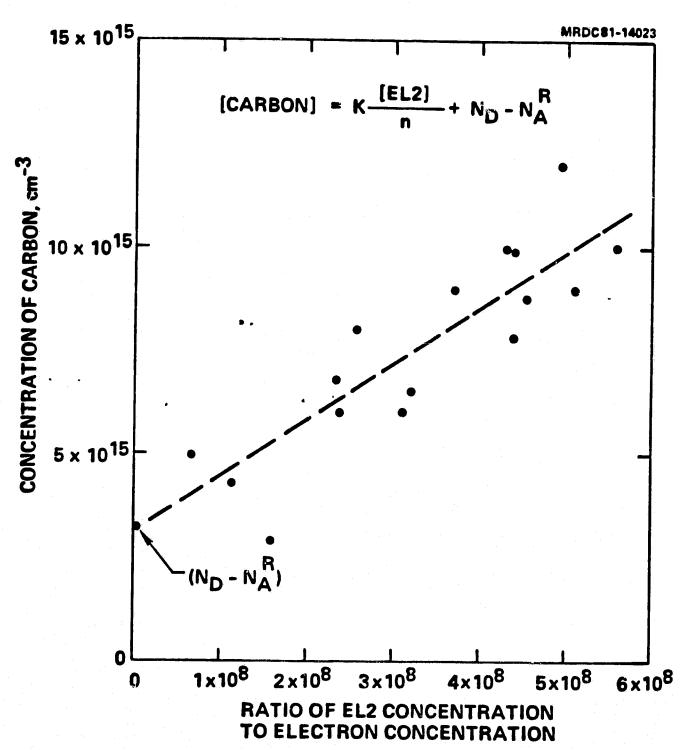


Figure 23

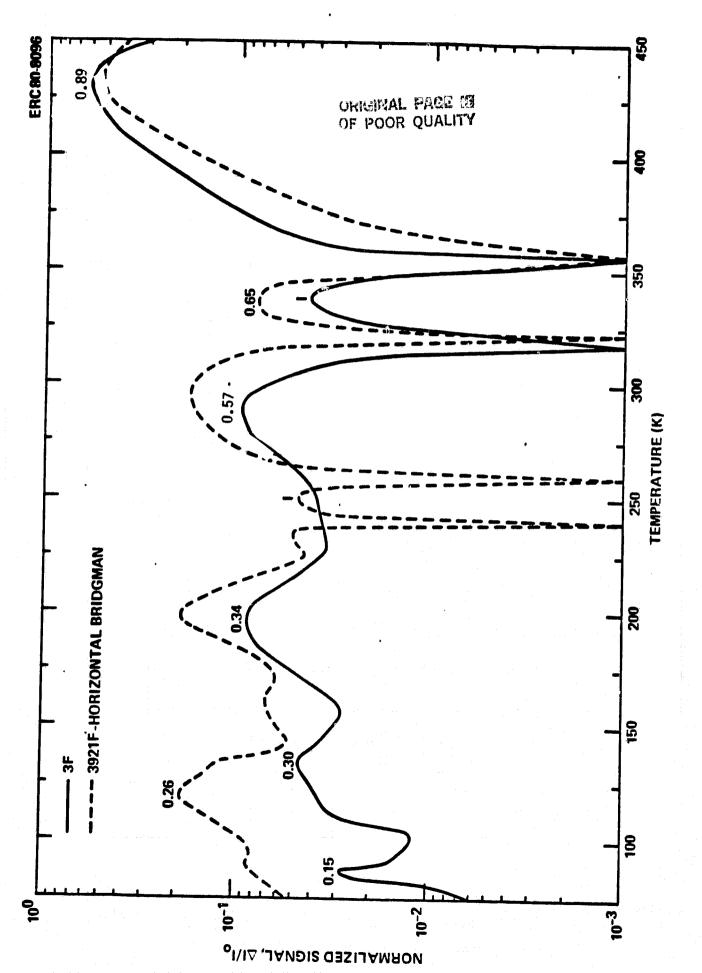


Figure 24

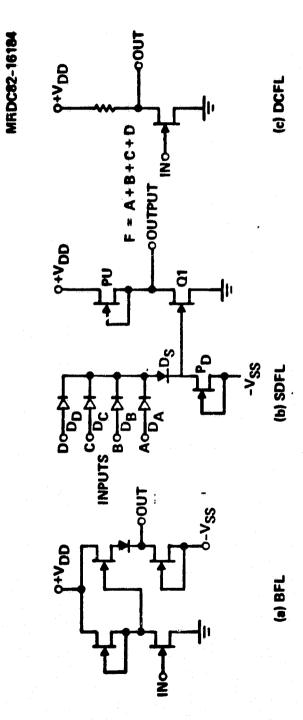


Figure 25

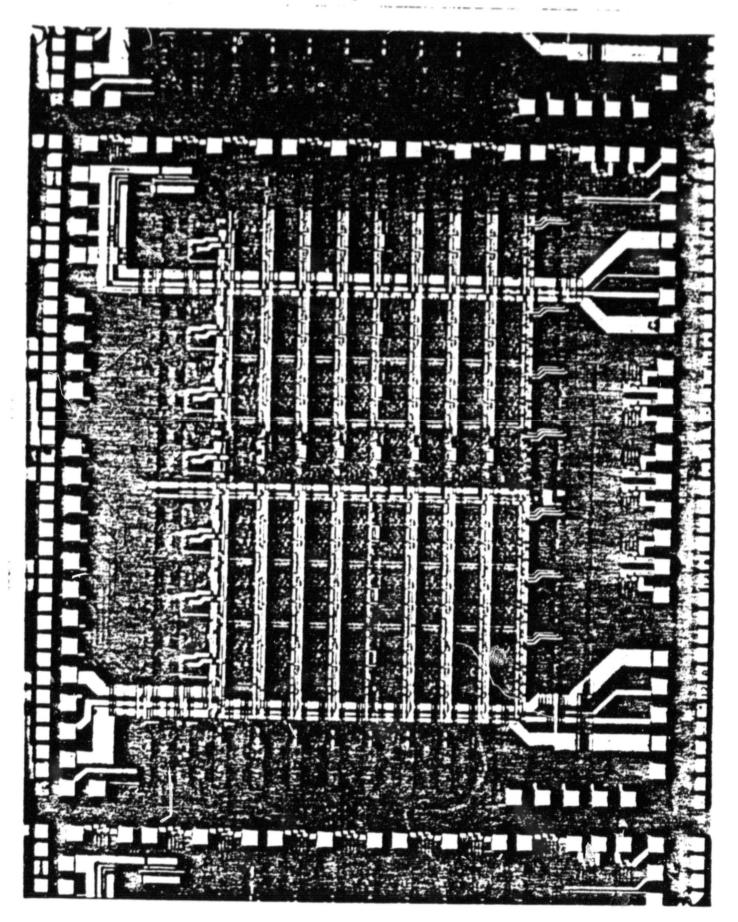


Figure 26

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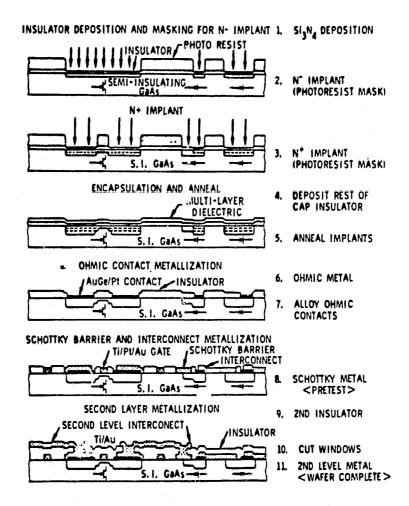


Figure 27

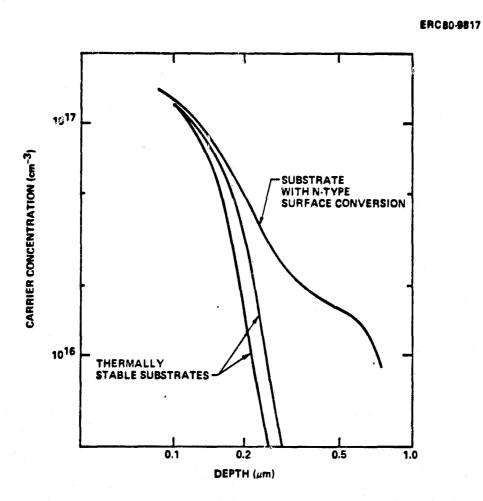
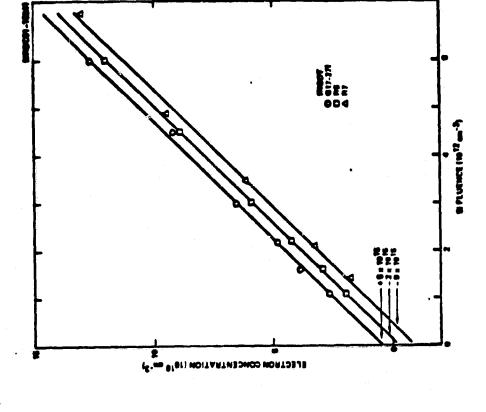


Figure 28



BANDC81-13342



DEPTH (pm)

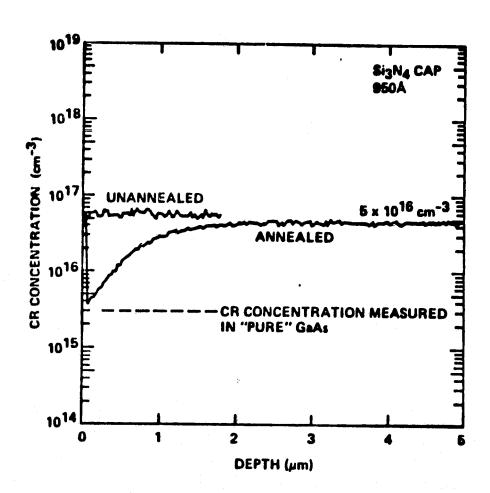


Figure 30

NUMBER OF INGOTS

NUMBER OF INGOTS

Figure 31

# ORIGINAL PAGE 12 OF POOR QUALITY

MRDC 81-15361

#### **DEPLETION VOLTAGE**

1.2 - 1.3 V

/ 1.3 - 1.4 V

O 1.4 - 1.5 V

Figure 32

# ORIGINAL PAGE IS OF POOR QUALITY

### MRDC83-20964

$$\overline{V}_{p}$$
 = 0.9441 V  
< $V_{p}$ > = 2.491 E-02(2.6%)

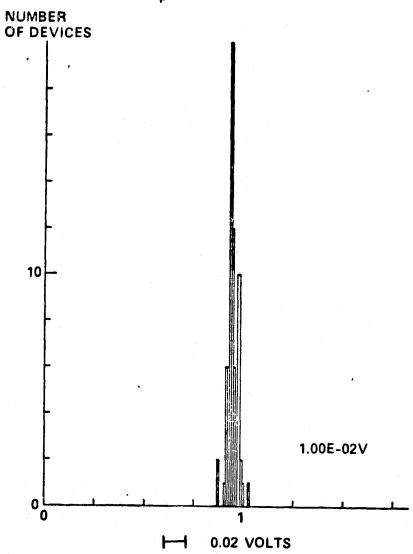


Figure 33

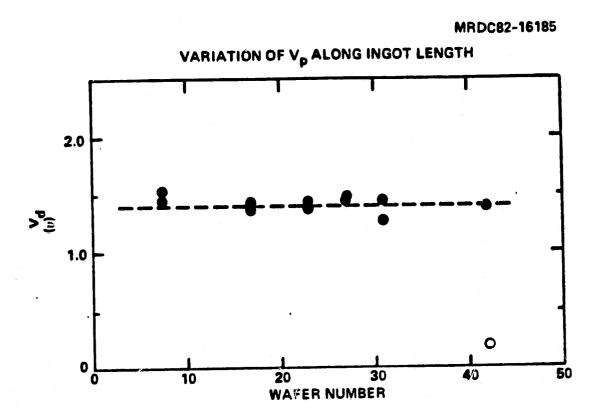


Figure 34